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Processor Architectures for *Y2K*

Klaus Waldschmidt
Bernd Klauer

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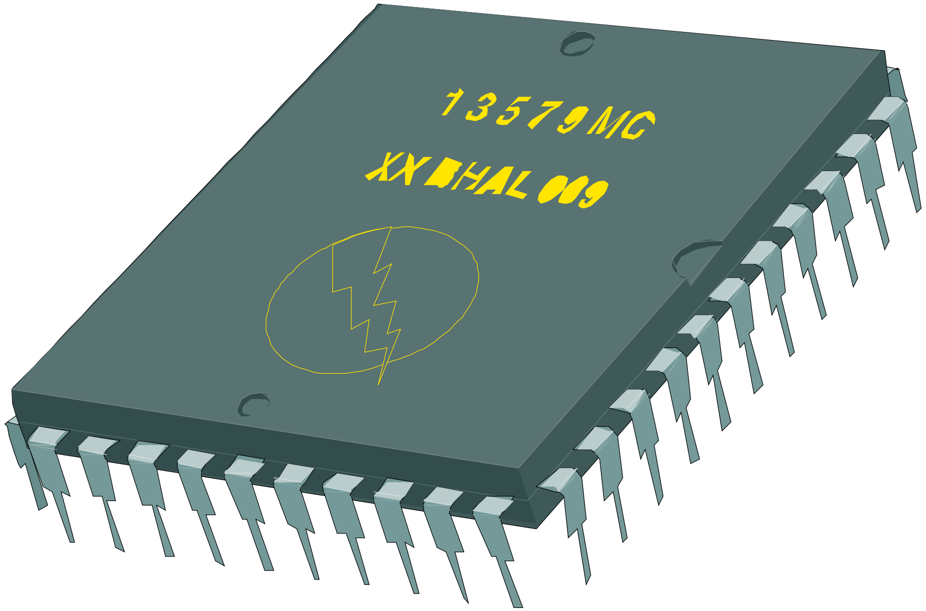
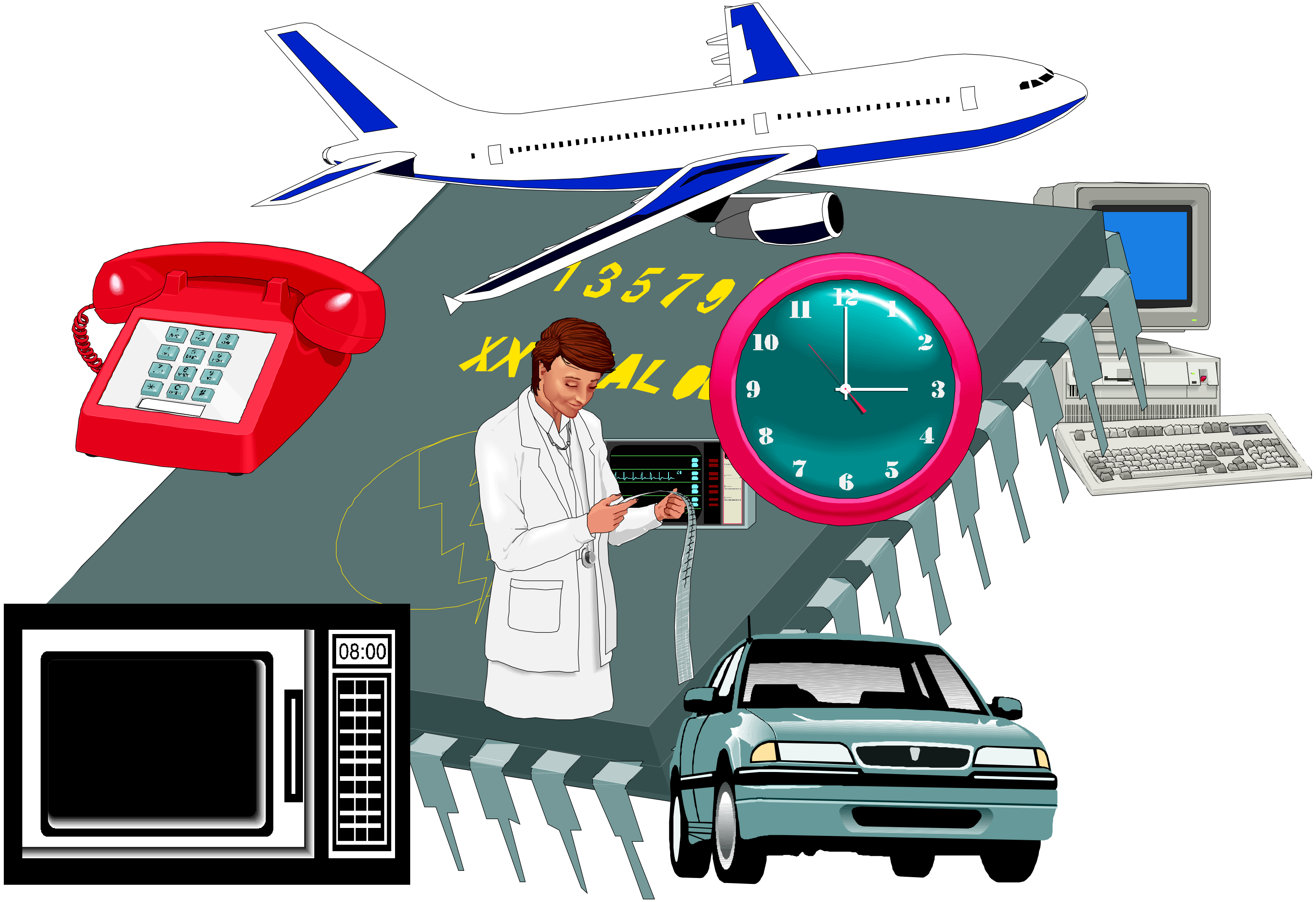
Microprocessors



- Core of modern analog and digital circuits
- Growing significance as performance indicator for VLSI technologies
- The technical component of the term *Information Society* is dominated by the microprocessor



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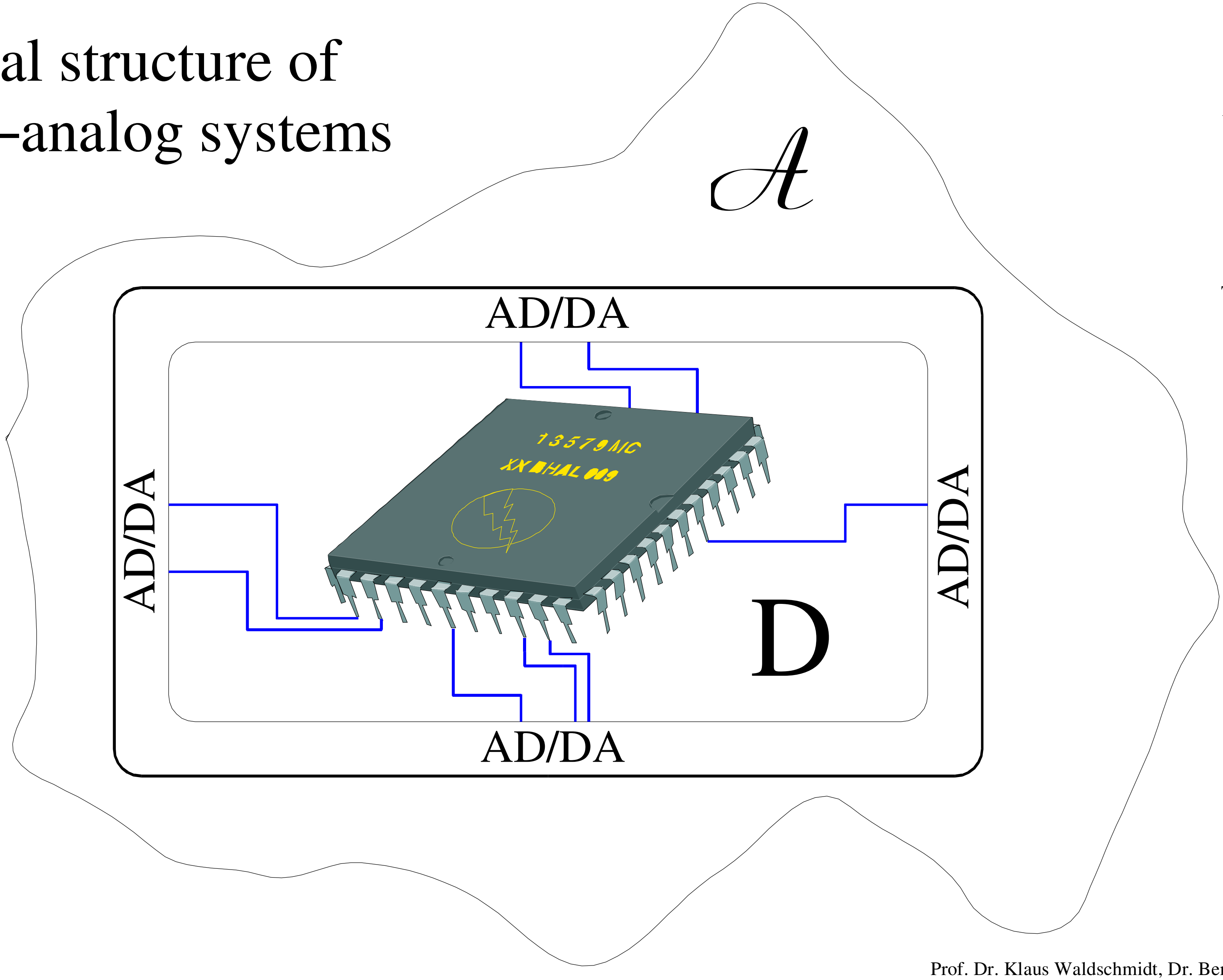
Prof. Dr. Klaus Waldschmidt, Dr. Bernd Klauer

Typical structure of quasi–analog systems



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Challenges
for the Y2K– processor architects

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- Technology
- Architecture
- Compilers
- Design

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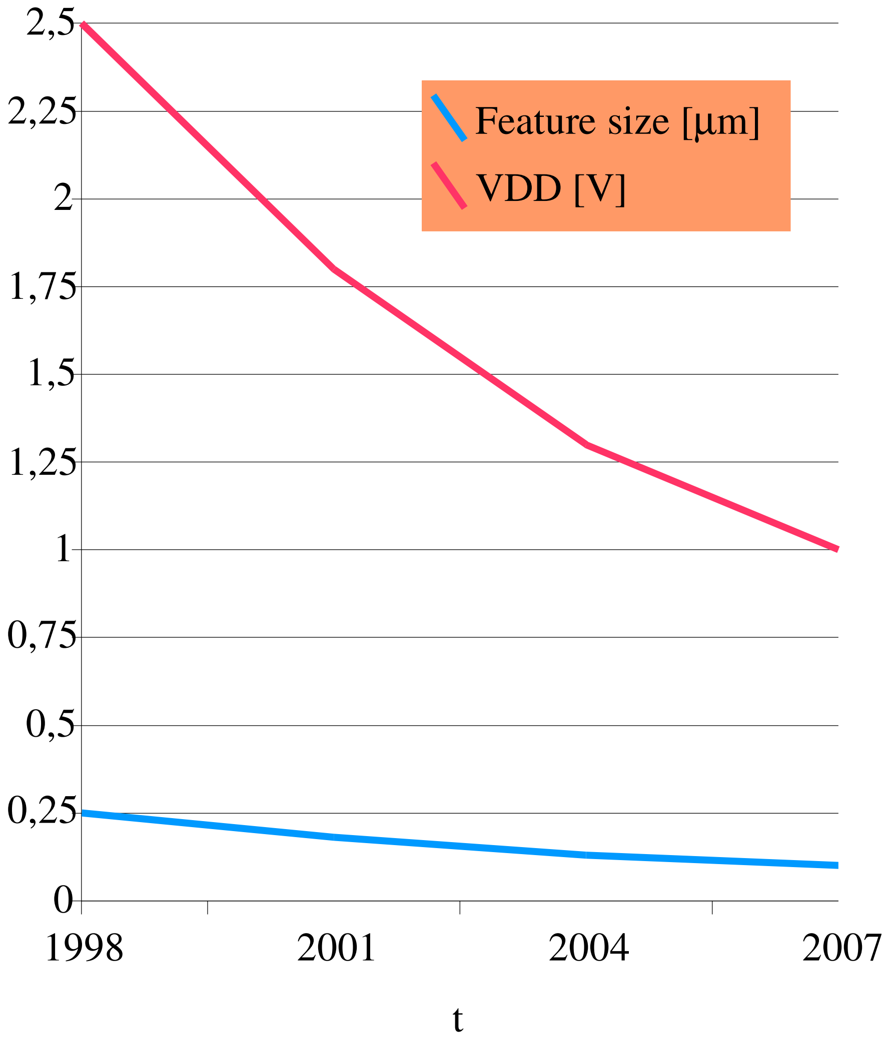
CMOS

- Copper on the metal layer
- Even better conductors as connections

Scaling



- Surface scales with $\frac{1}{c^2}$
- Switching time of active components scales with c
- Constant scaling of signal propagation delays

- Computation times are dominated by signal delays
- Connection oriented design replaces logic oriented design

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Chip size, circuit size, clock and power

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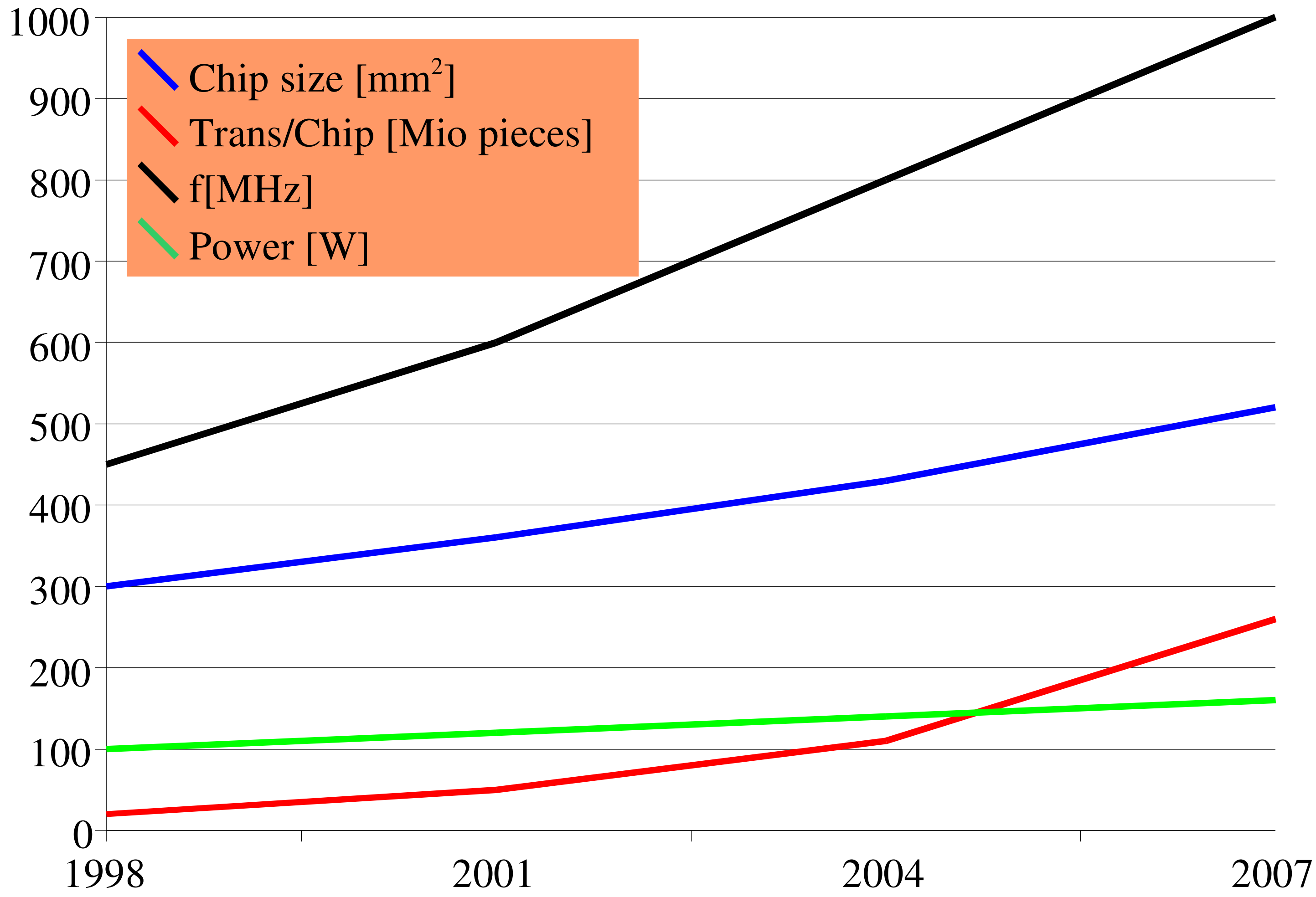

The technology (money) wall

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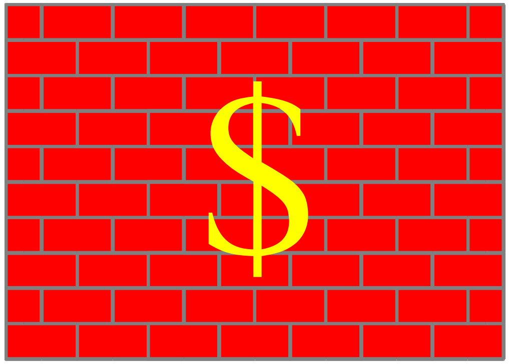
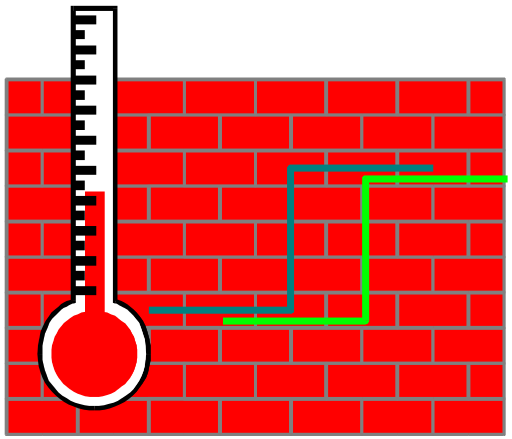
- Lithographic projections do not allow for feature sizes smaller than 0.1µm
- Circuits with 500 mm^2 have an average fault rate of 1 under modern clean room conditions



- Increasing costs
- Decreasing output

Clock ...



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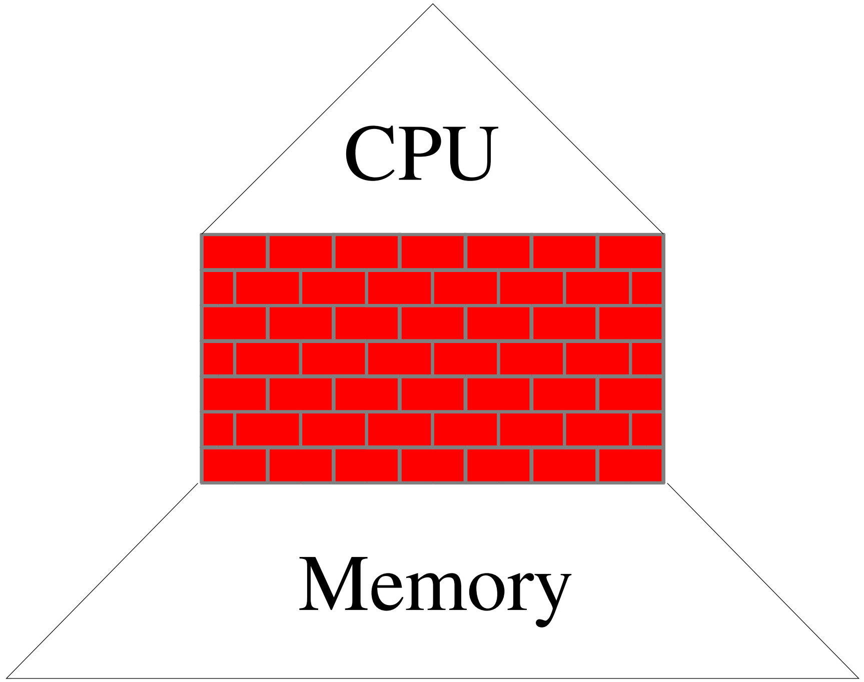
- The supply voltage cannot be reduced under 1V by technical reasons

- With a clock rate of 10GHz light propagates about 3cm within 1 clock cycle in a vacuum. In semiconductors light propagates with 1/10 of the speed in a vacuum (3mm). At 10GHz we have 10 clock cycles on a 3cm connection

▶ Thermal problems

▶ Shifting of clock phases has to be considered in future designs

The memory wall



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- Memory capacity scales with the square of the chip size with constant access time
- Caches cannot close the memory gap due to the restricted locality of typical programs

▶ Increasing clock rates cause an increasing memory gap

▶ Increasing clock rates return only low gains in computing time

Architecture ...

The types of architecture are established not by architects but by society, according to the needs of the different institutions. Society sets the goals and assigns the architects the job of finding the means of achieving them.

(Ecyclopedia Britannica)

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Structure of modern Microprocessors

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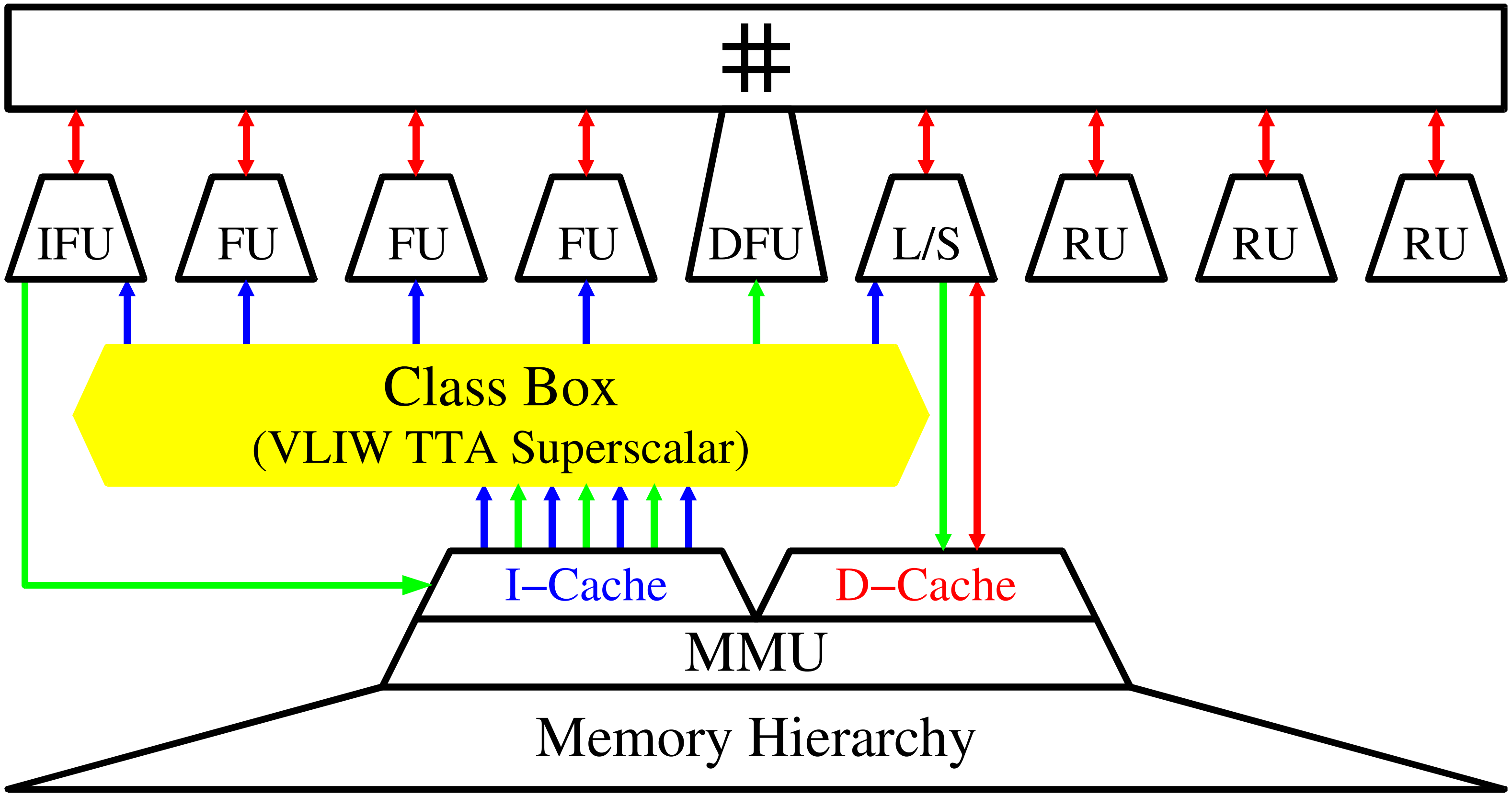

VLIW Architectures

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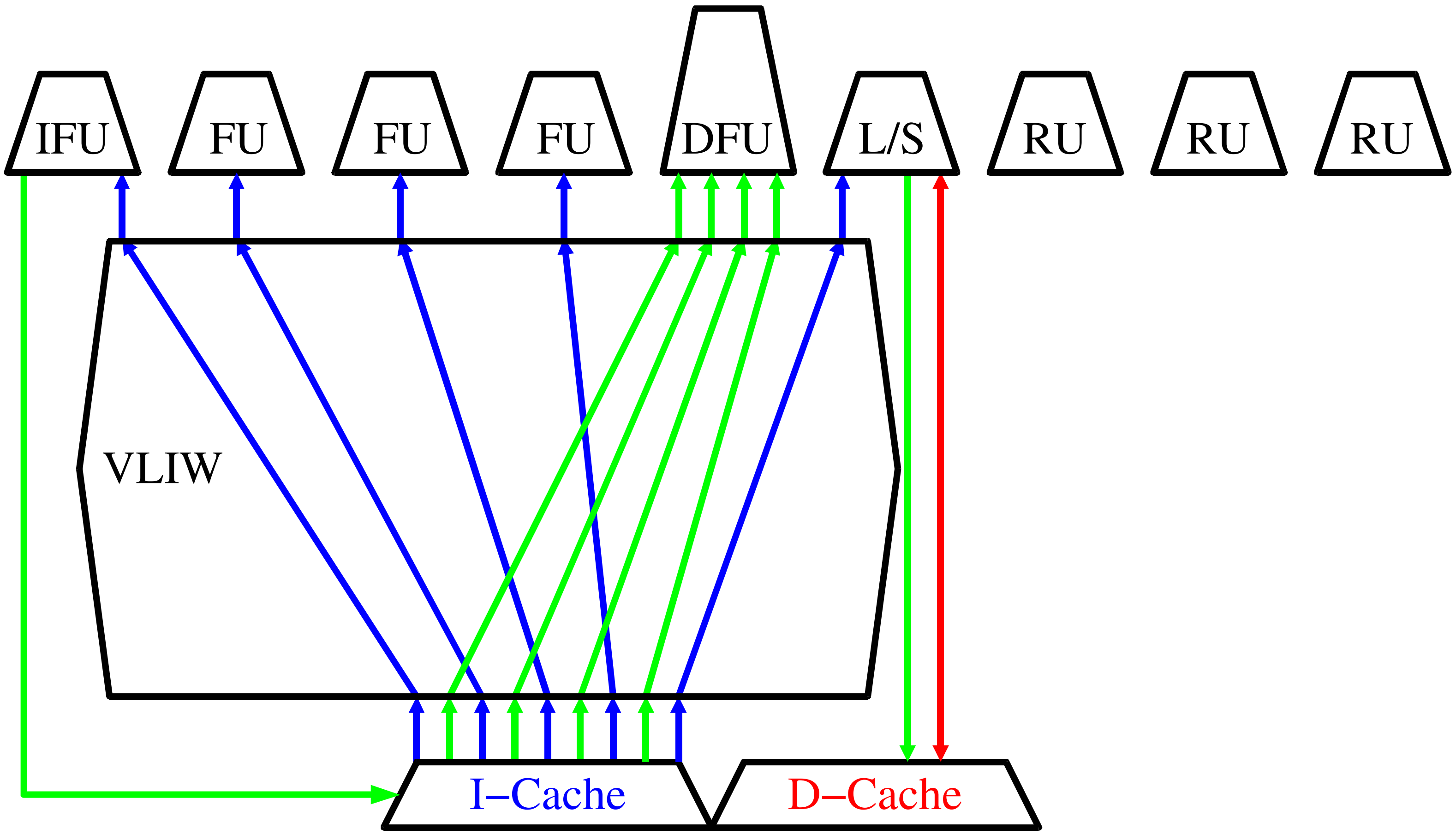

Superscalar Architectures

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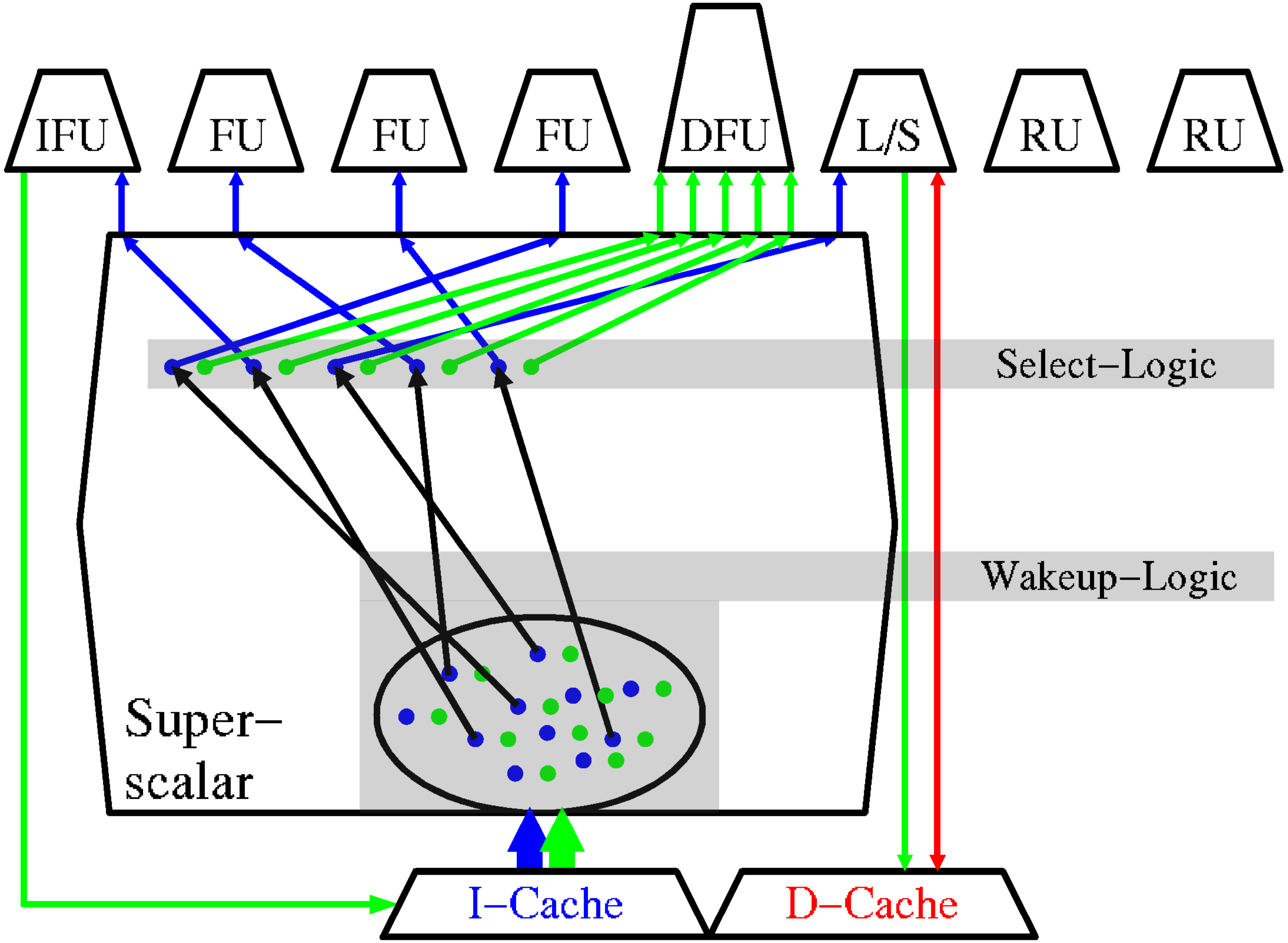
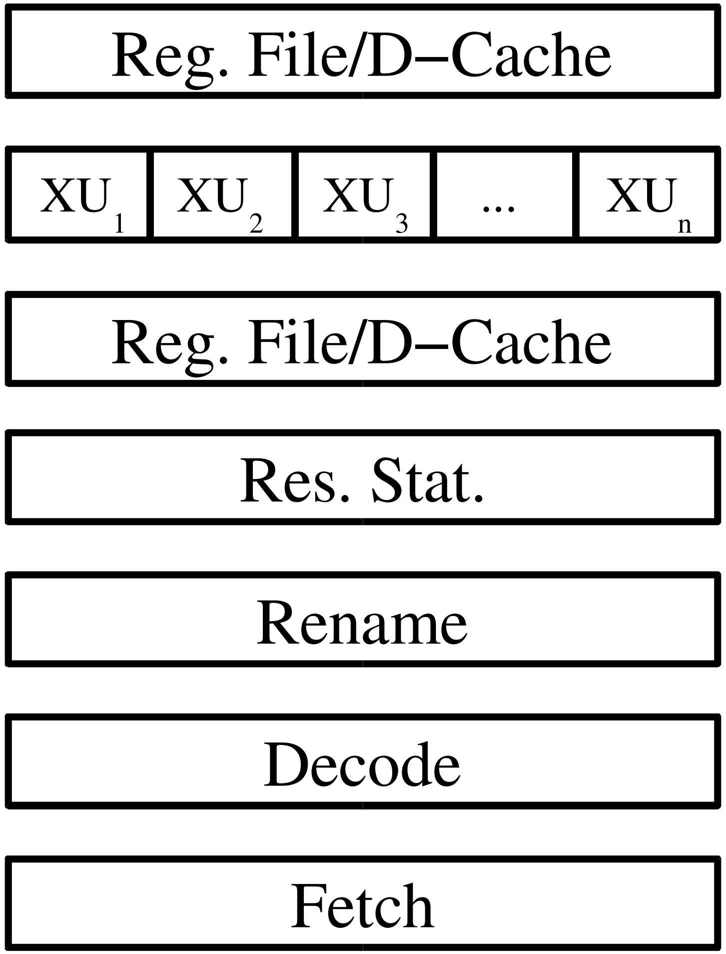


out–of–order execution by dataflow analysis

Superscalar pipeline



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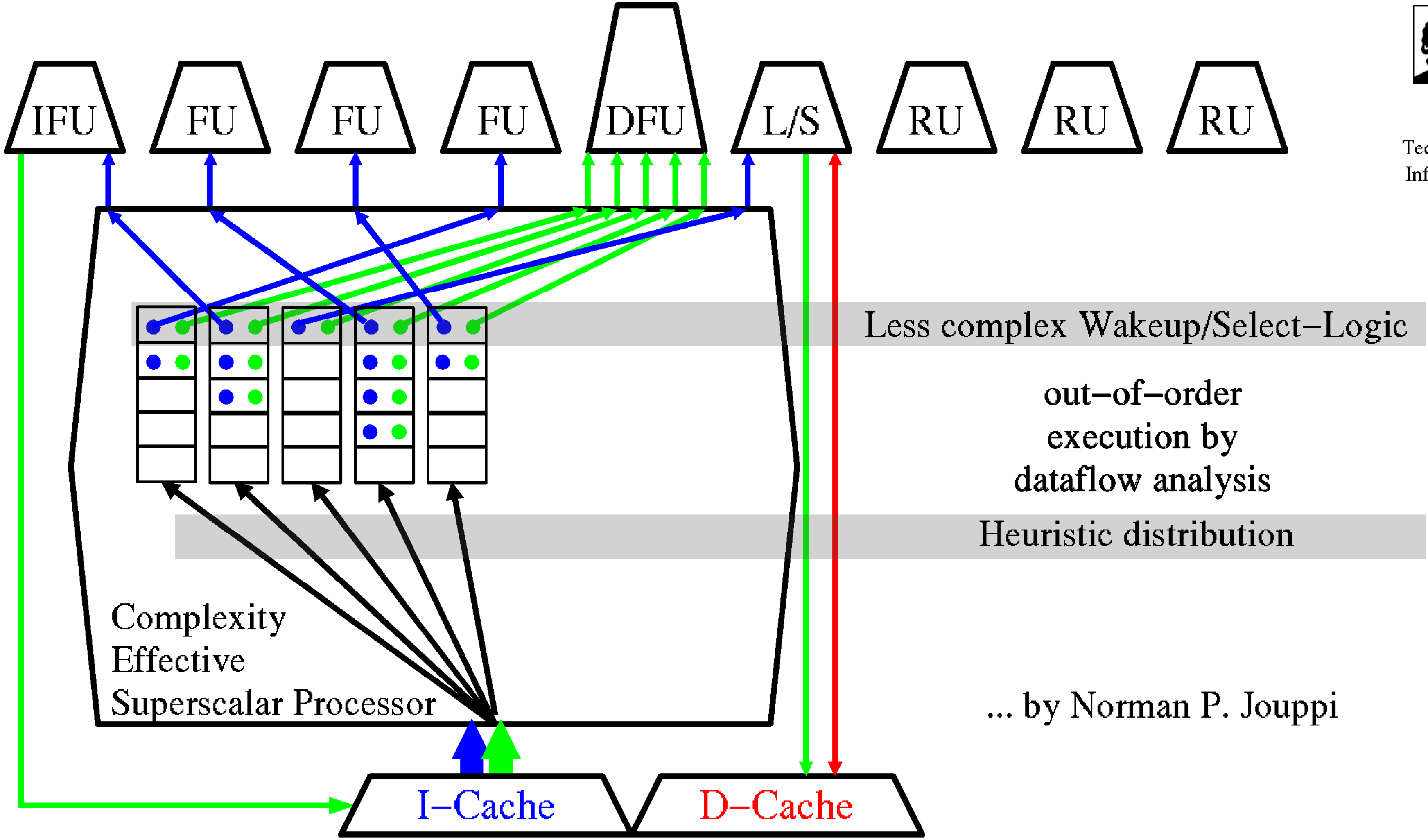

... by Norman P. Jouppi

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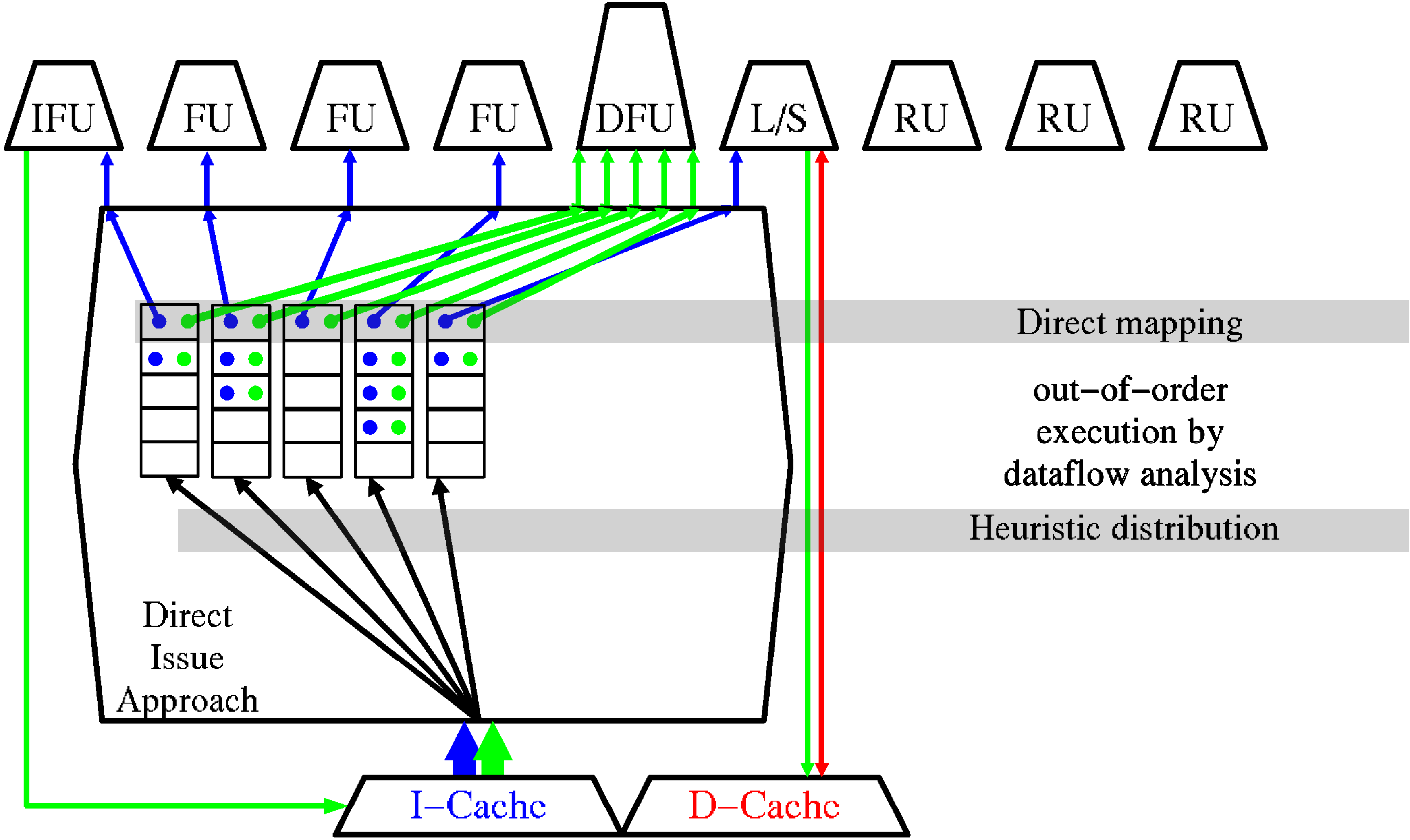

TTAs

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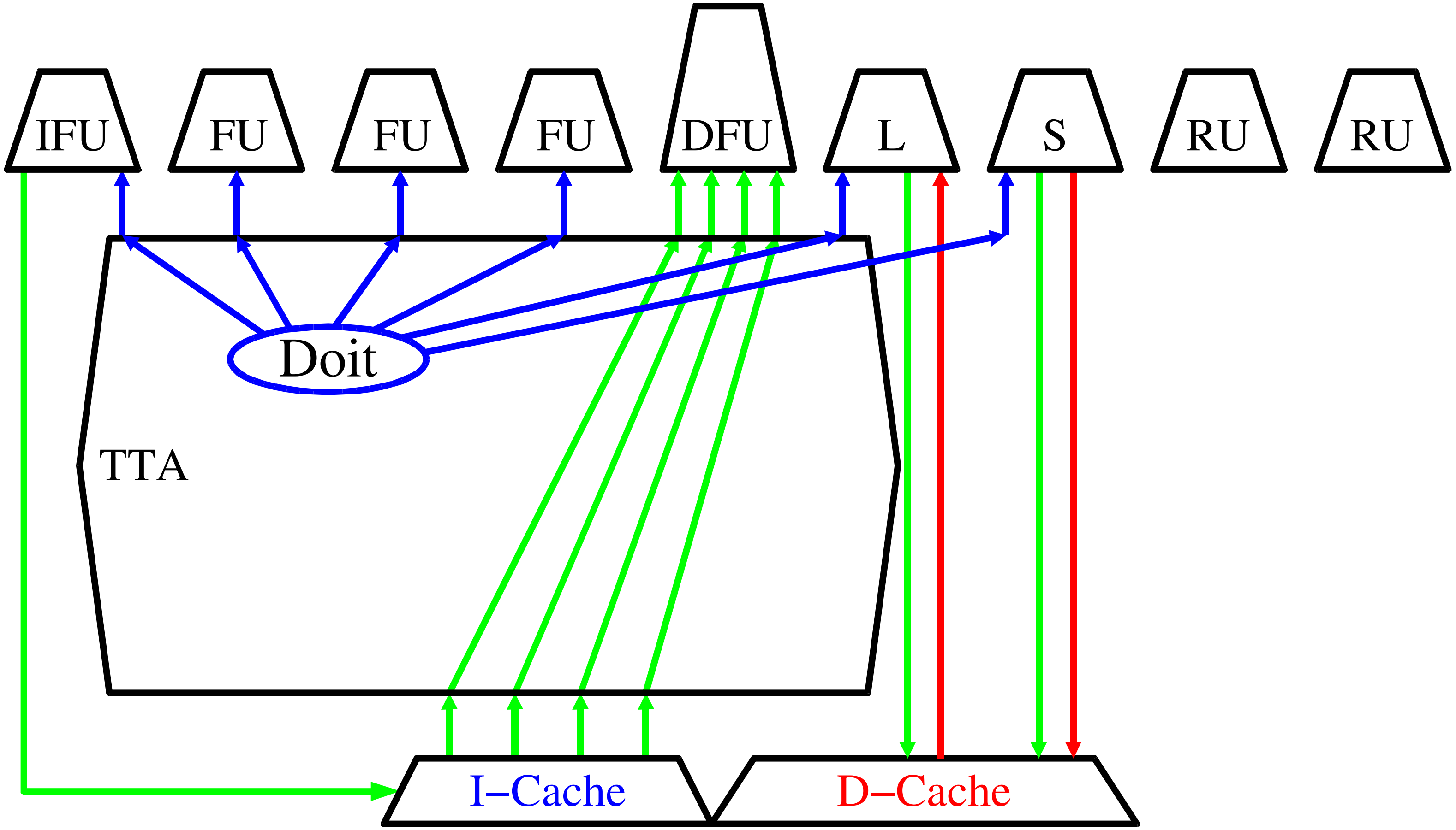

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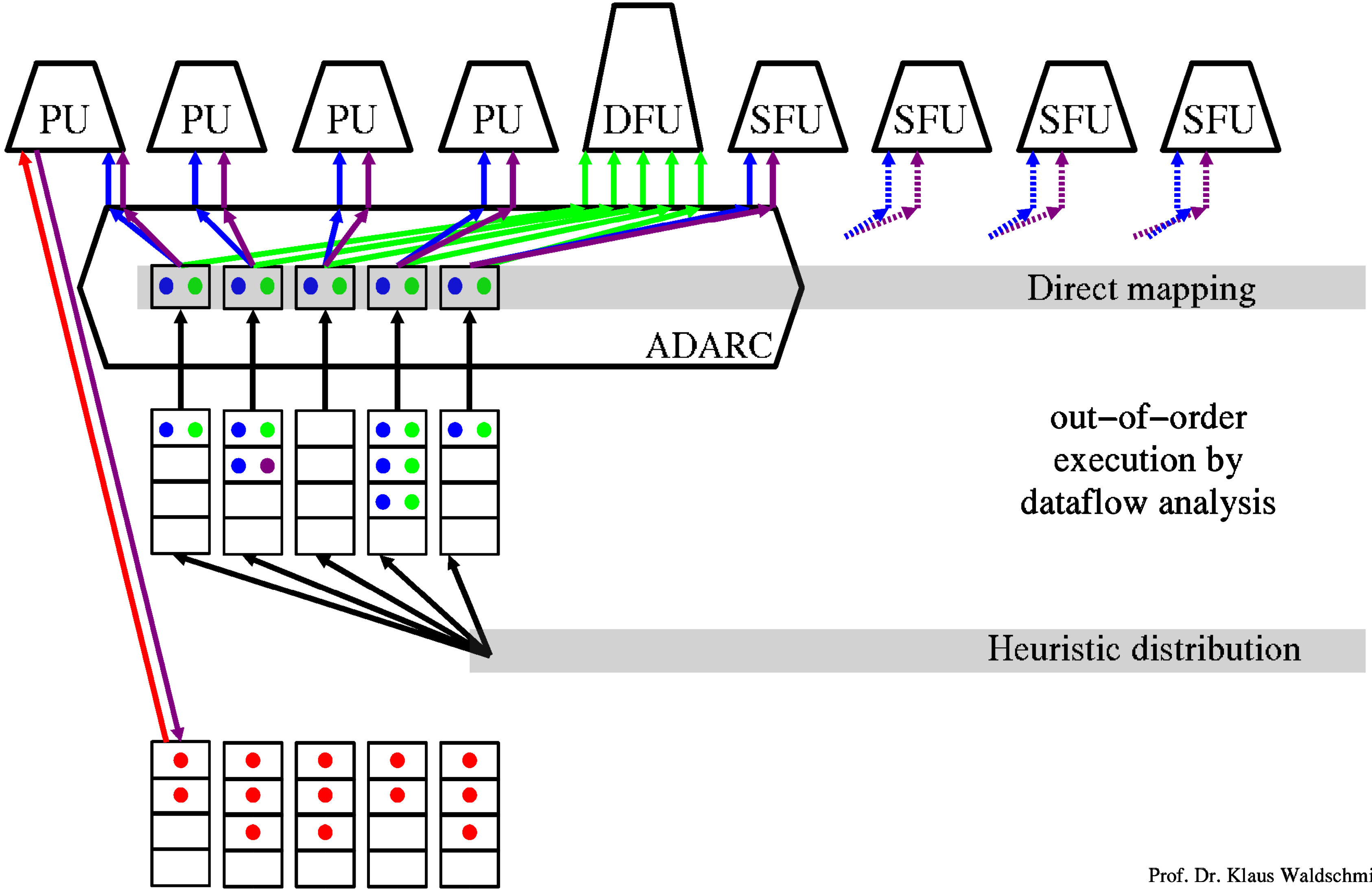

Bottlenecks

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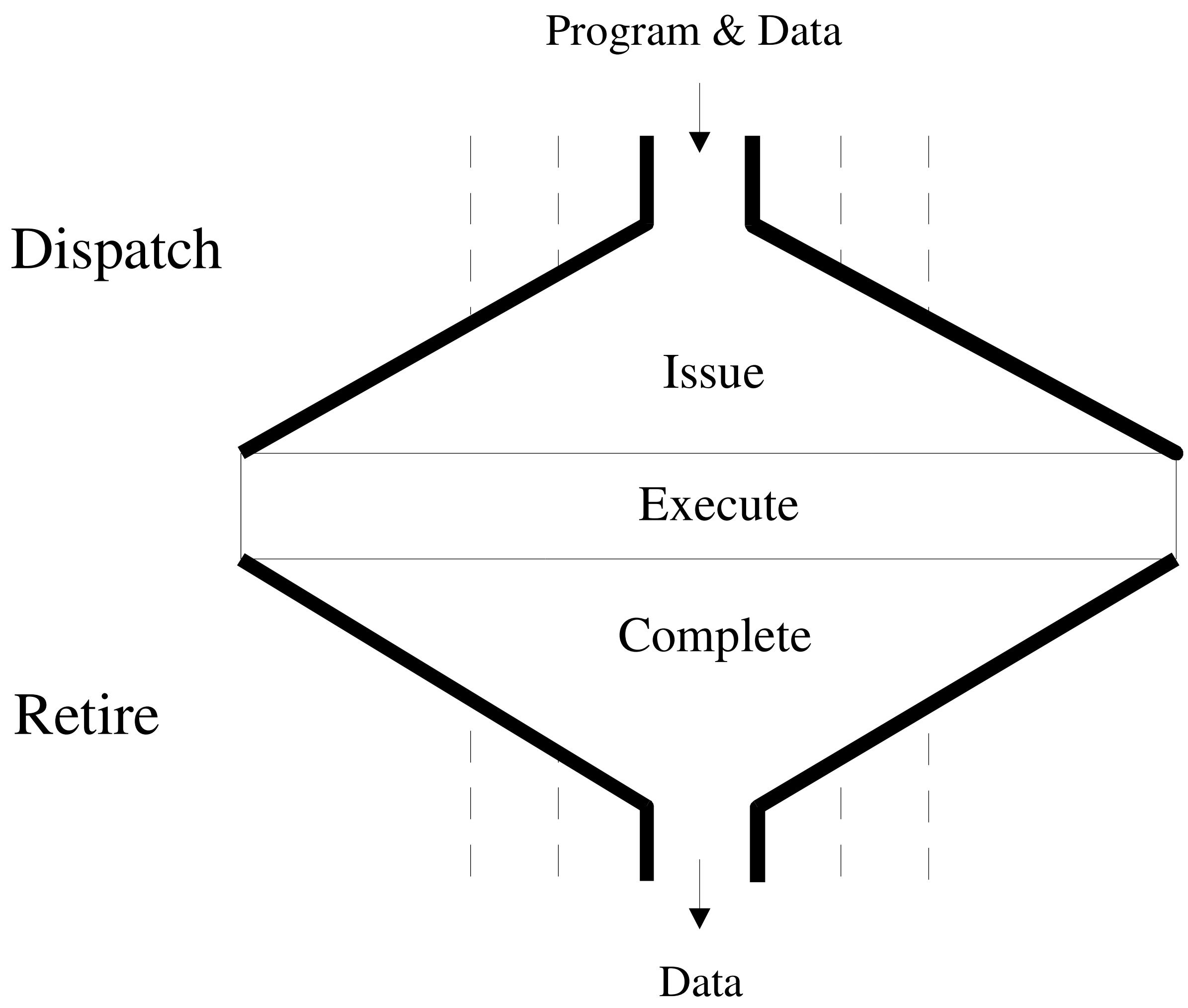

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Jahr	Chip size [mm ²]	Trans/Chip [Mio]	f [MHz]	Power [W]	Feature size [µm]	Spannung [V]
1998	300	20	450	100	0,25	2,5
2001	360	50	600	120	0,18	1,8
2004	430	110	800	140	0,13	1,3
2007	520 (1000)	260	1000	160	0,1	1
2012			10000		0,05	

SIA Roadmap 1994

c´t 17/99

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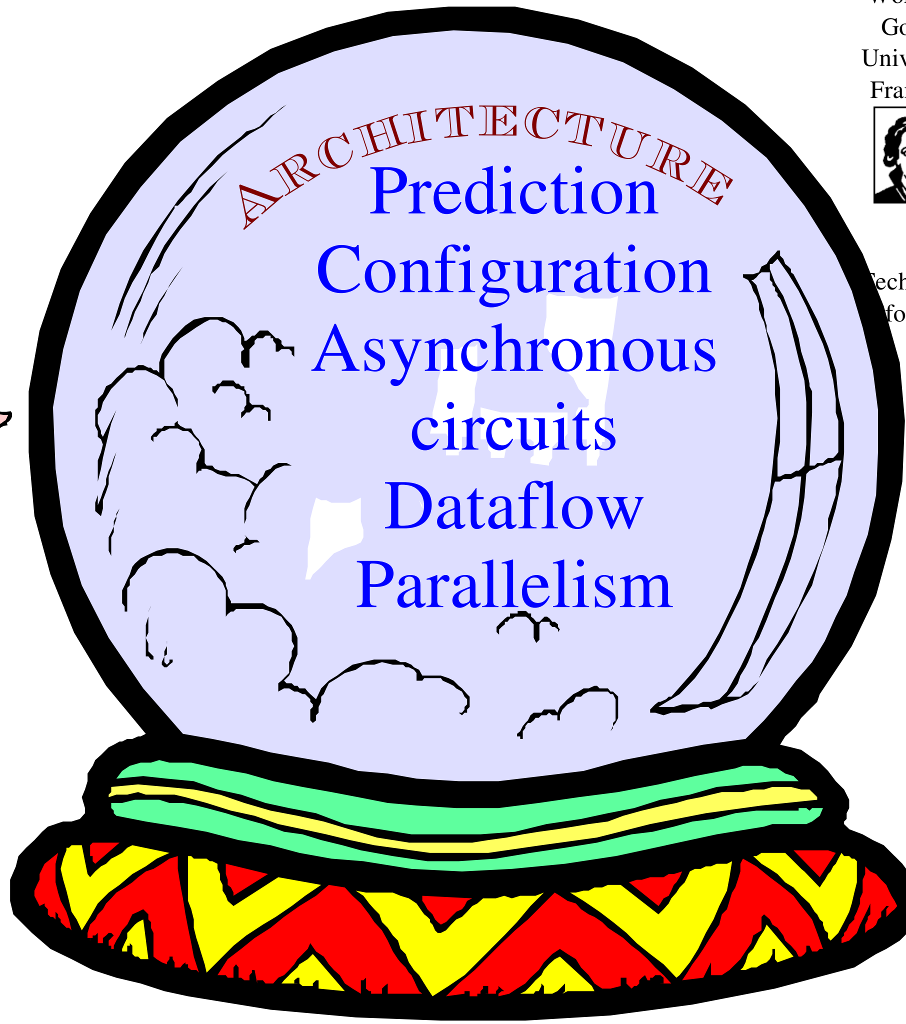

Prediction

- Early estimations of control flow decisions
- Early updating of the memory hierarchy concurrently with the program flow to minimize cache misses

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Configuration

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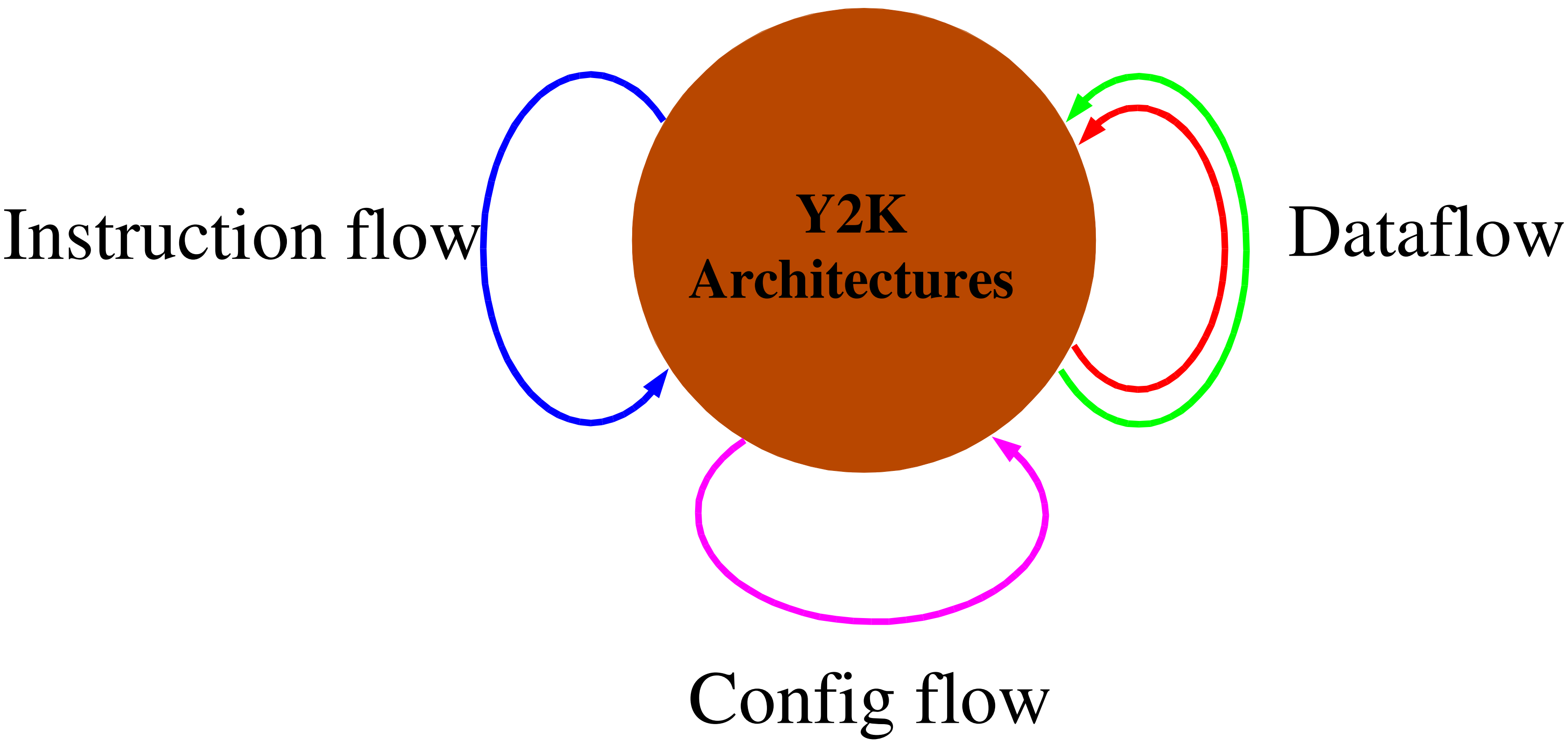

Config flow

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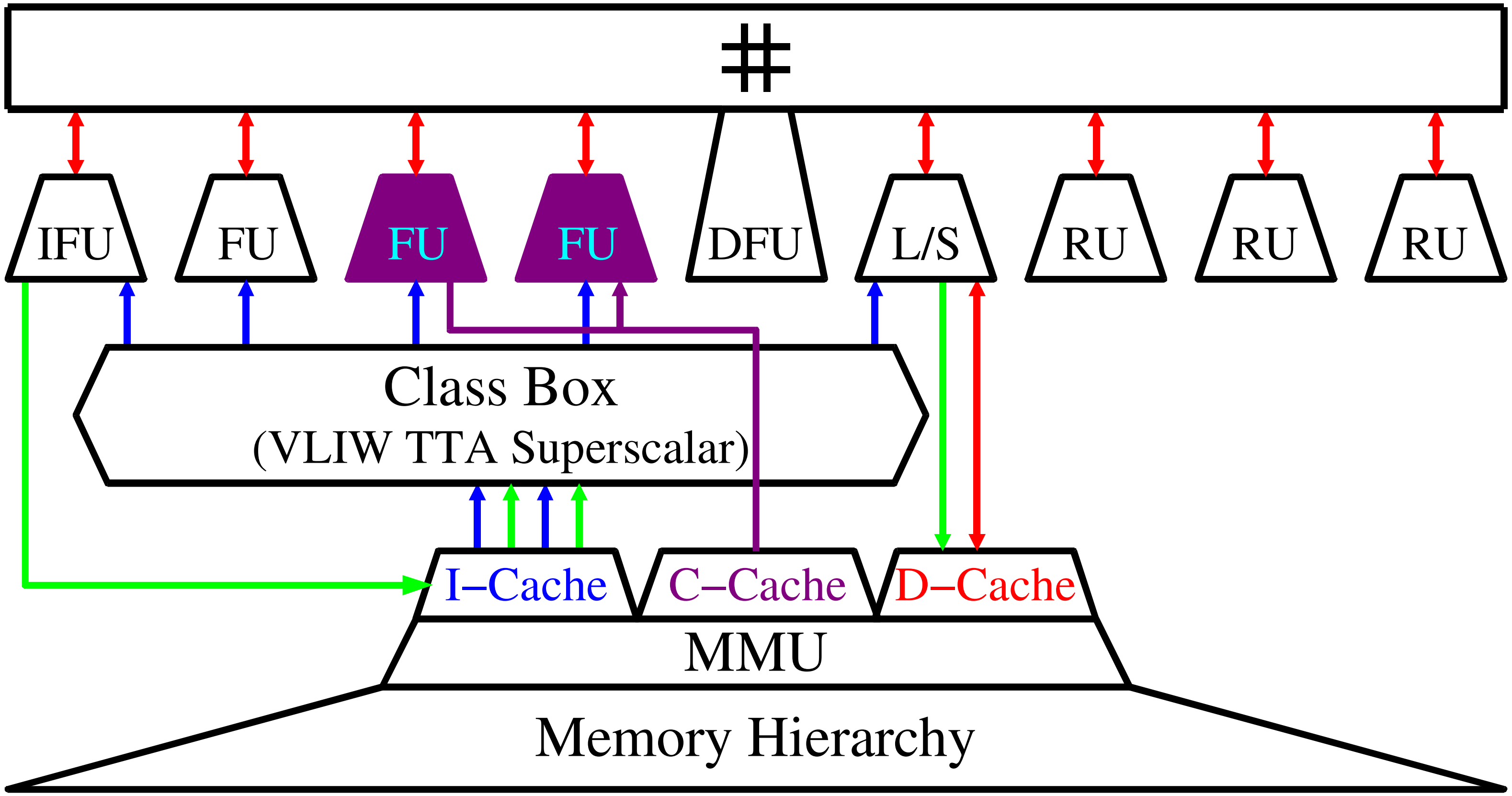

Config flow

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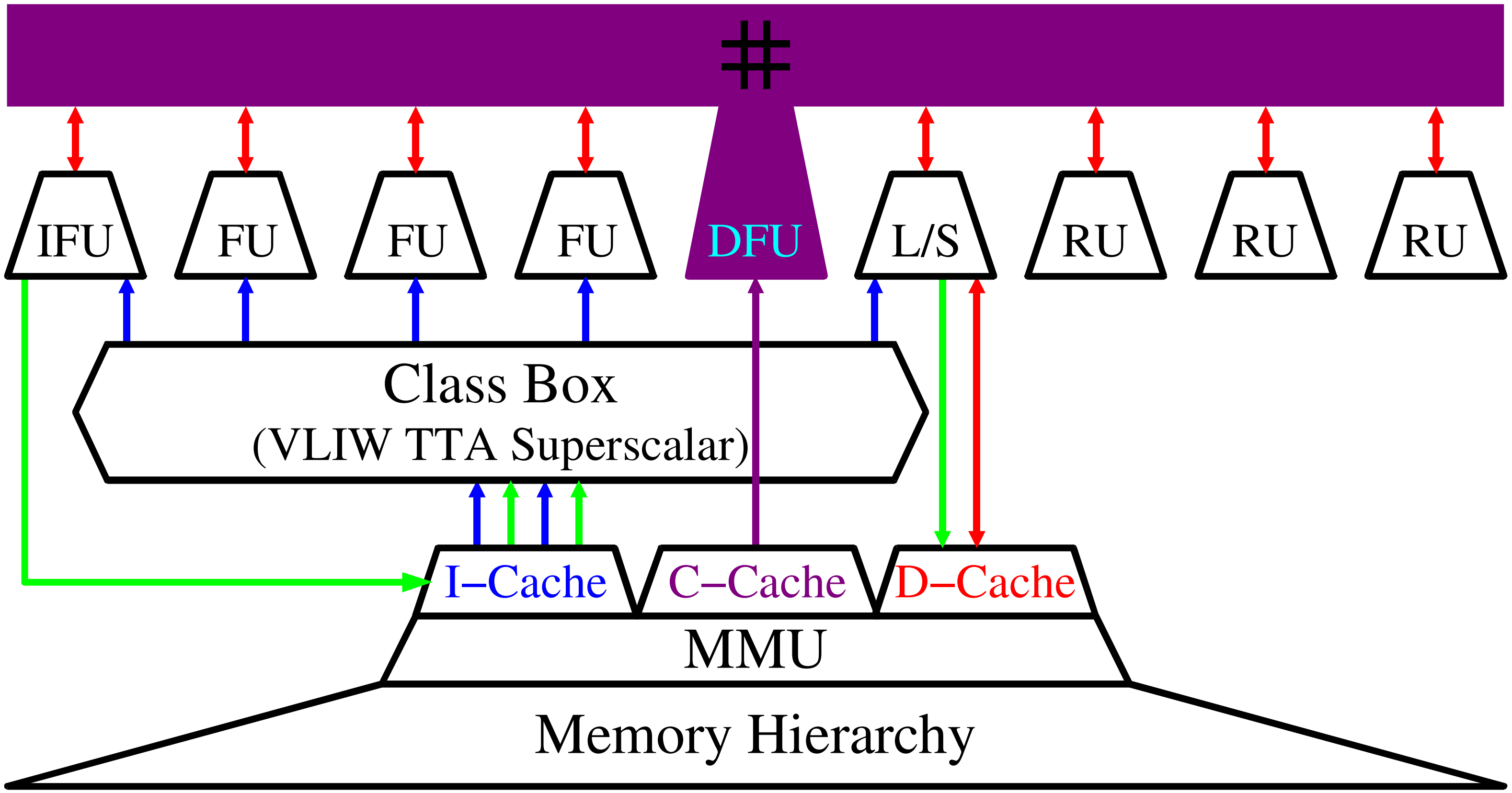
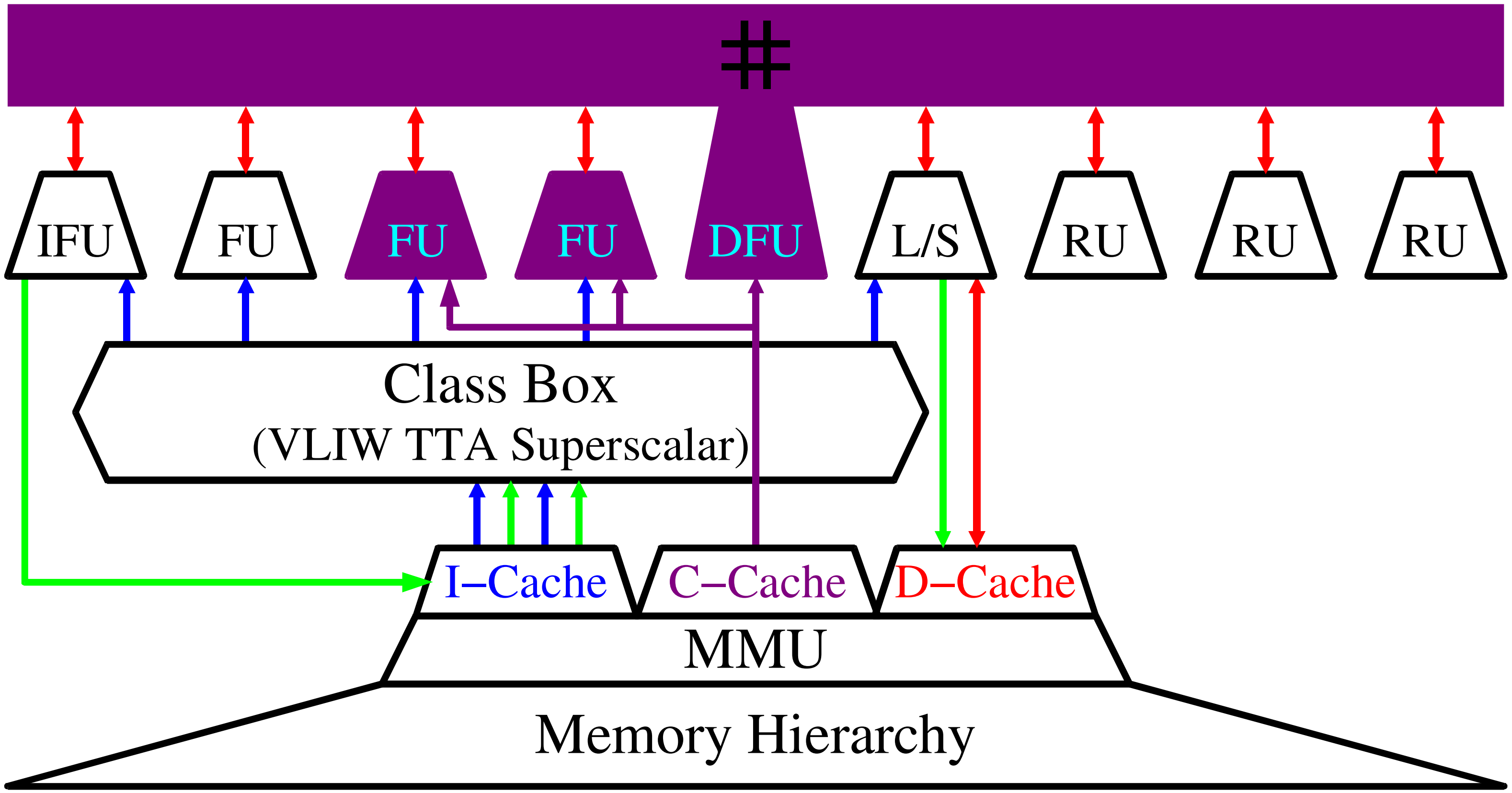


Config flow



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Parallelism

- configurable (asynchronous ?) multiprocessors
- medium or coarse grain prallelism e.g. threads or microthreads

- **cooperative load balancing at run time**

Load

Memory

Quality

Cooperative load balancing

Efficiency

Scalability

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Configuration
by programing languages/compilers

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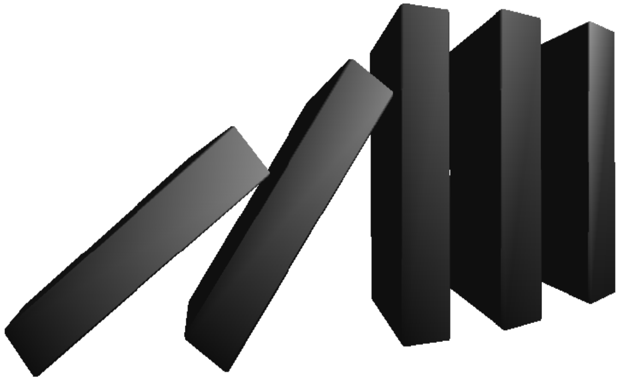
- explicitly by linguistic concepts in programing languages
  - Declarations
  - Procedures
  - Descriptions (direct circuit descriptions or embedding of HDLs e.g. VHDL)
- automatically by a compiler (data path analysis)

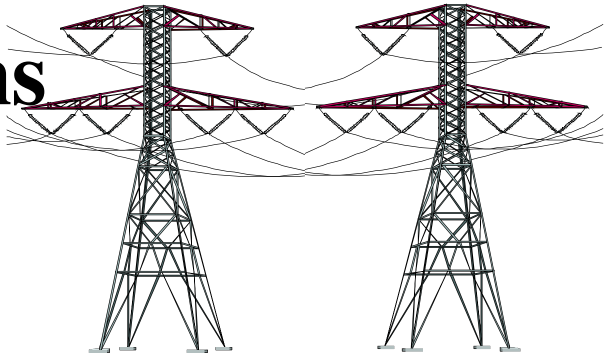

DESIGN
Optimization
of connections
Asynchronous
components

Design

- To master designs with more than 20 (100) Mio transistors ✓199x
- Logic optimization ✓ 199x
- **Mastering of asynchronous circuits**



- **Optimization of connections and power**



- **Primary & Secondary effects**

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