



Heriot-Watt University
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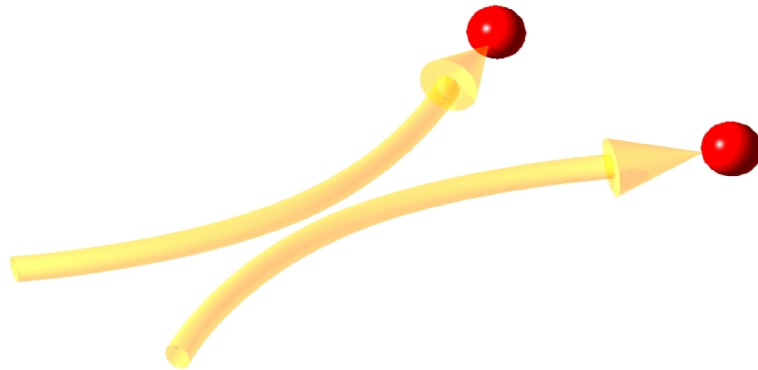
Optoelectronics in the Reconfigurable Environment

(An Overview of Optics in Computing)

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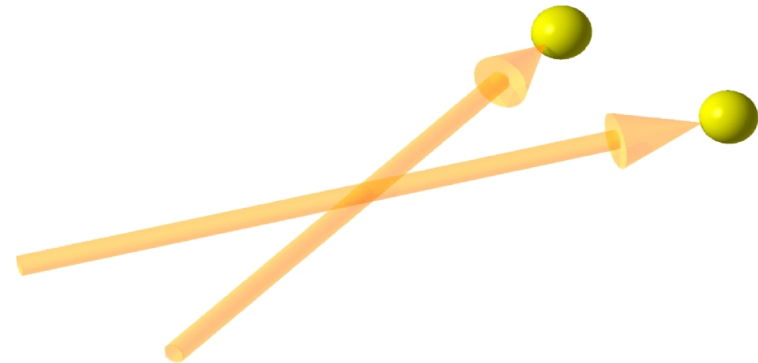
Optoelectronic Interconnects

Electrons



Since electrons carry mass and charge they interact strongly (Coulomb Interaction). Ideally suited for switching.

Photons

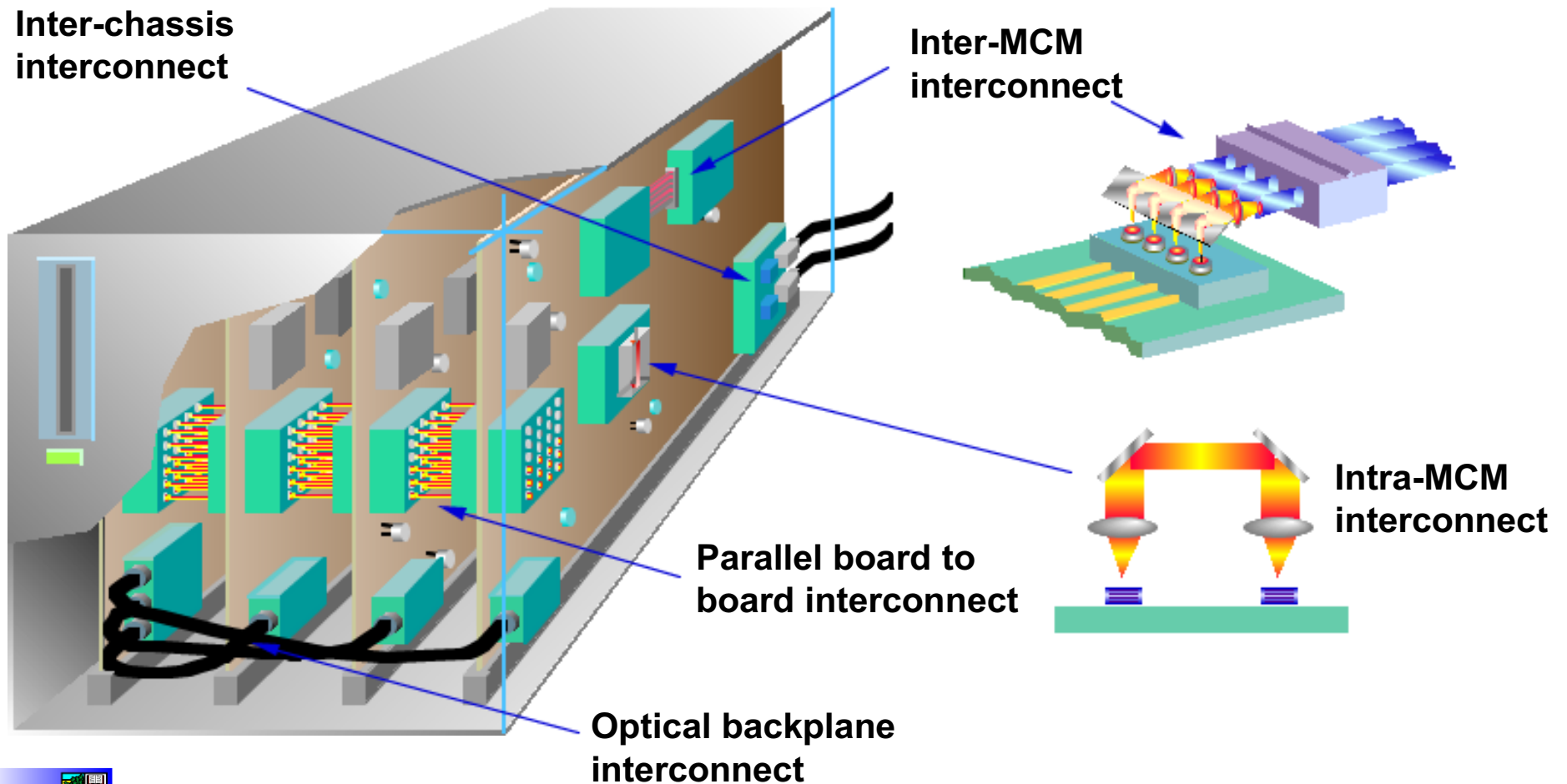


Photons do not carry mass or charge and are non-interacting in free space. They are ideally suited to interconnection.



Optical Interconnection

Sample uses of optical interconnection in an MCM (Multi-Chip Module).



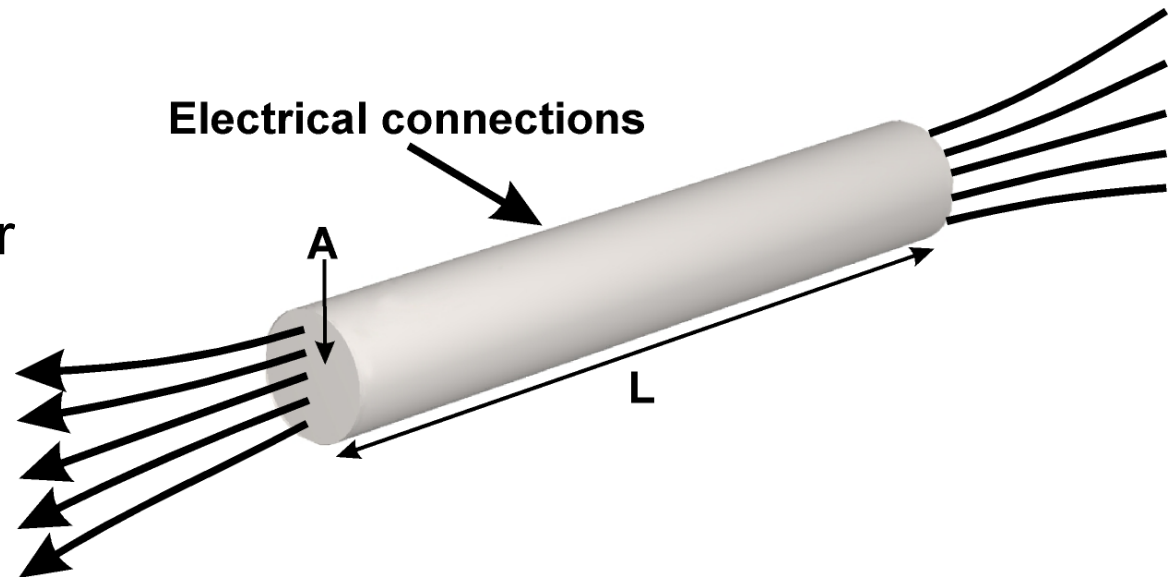
(Maria Kufner, Vrije Universiteit Brussel.)

Bandwidth Limitations

The maximum bandwidth of electronic systems has been estimated by Burton Smith (Tera Corp.) and David Miller (Bell Labs) as:

$$B_{\max} = 500 \cdot \frac{A}{L^2} \text{ THz}$$

Aspect ratio



Consider chip connections for a 10x10mm chip (100mm²):

- Edge connections: 400 with ~100μm diameter lines A=3mm²
- 2D Solder Bump array: 2,000 with ~15μm diameter pads A=3mm²

Thus for a 10cm electrical connection across a board $B_{\max} \sim 150\text{GHz}$



SIA Roadmap

I/O figures for high performance ASIC systems taken from Semiconductor Industry Association.

Year	1999	2002	2005	2008	2011	2014
Process size (nm)	180	130	100	70	50	35
Chip size (mm ²)	450	509	622	713	817	937
On-chip clock (GHz)	1.2	1.6	2.0	2.5	3.0	3.6
I/O Bus speed (MHz) [†]	480	885	1035	1285	1540	1800
I/O Pads ^{††}	368	464	584	736	927	1167
Off-chip data rate (Gbs ⁻¹)	177	410	604	946	1428	2100

[†] Chip to board (off-chip) speed (high performance for peripheral buses.

^{††} Chip to package pads (peripheral).



The Attraction of Optics

- **Off Chip Data Rates:** Currently we can drive 4,096 channels from 1cm^2 and see no real obstacle to reaching $>10,000$ channels.
- **Bandwidth in Busses:** A 1cm^2 relay can carry $>100,000$ channels. Currently we are driving at 200MHz giving a bandwidth of approximately 20Tbs^{-1} . Devices may be driven at 10Gbs^{-1} so the relay can handle $1,000\text{Tbs}^{-1}$ if we are not CMOS limited (the theoretical limit is actually much higher).
- **Pin-Out Limitations:** The physical pin-out limit can be overcome with additional optical pins.



The Attraction of Optics

- **Data Acquisition:** The naturally parallel nature of the connections implies high parallelism around any machine: e.g. to and from memory and peripherals.
- **Distance:** Optical signal transmission lengths of the order of meters are attainable without a significant increase in driving power.
- **Power Consumption:** Off-chip optical interconnection uses less power in comparison to electronics.

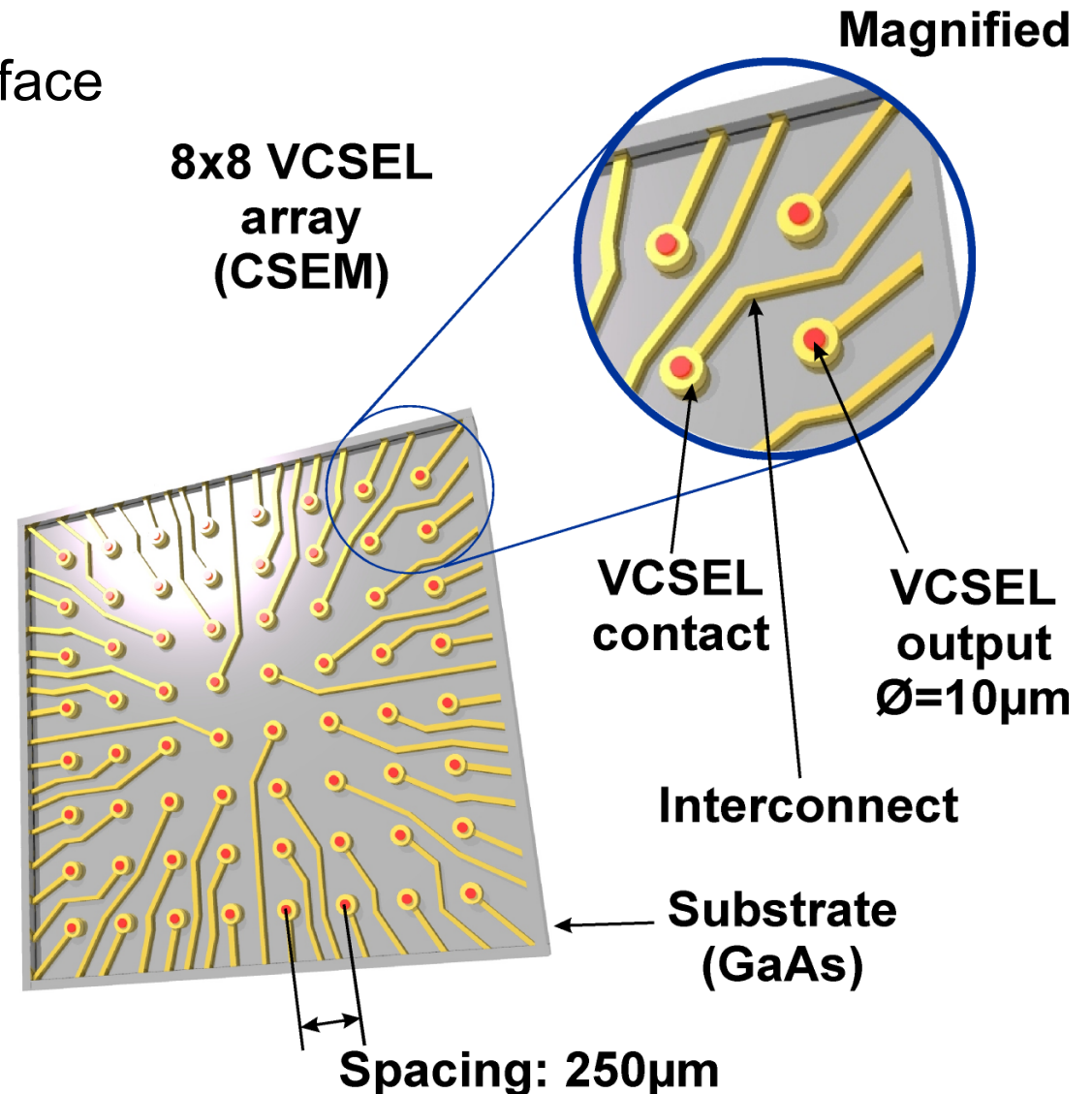
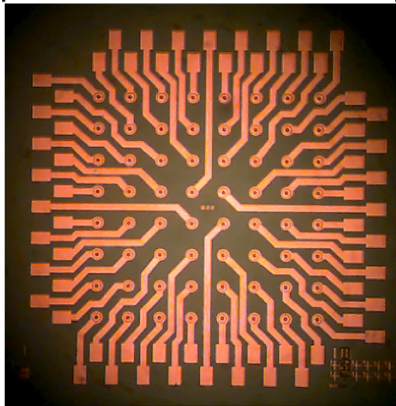


The VCSEL Array

The VCSEL (Vertical Cavity Surface Emitting Laser) is a laser diode that emits from the surface of the substrate.

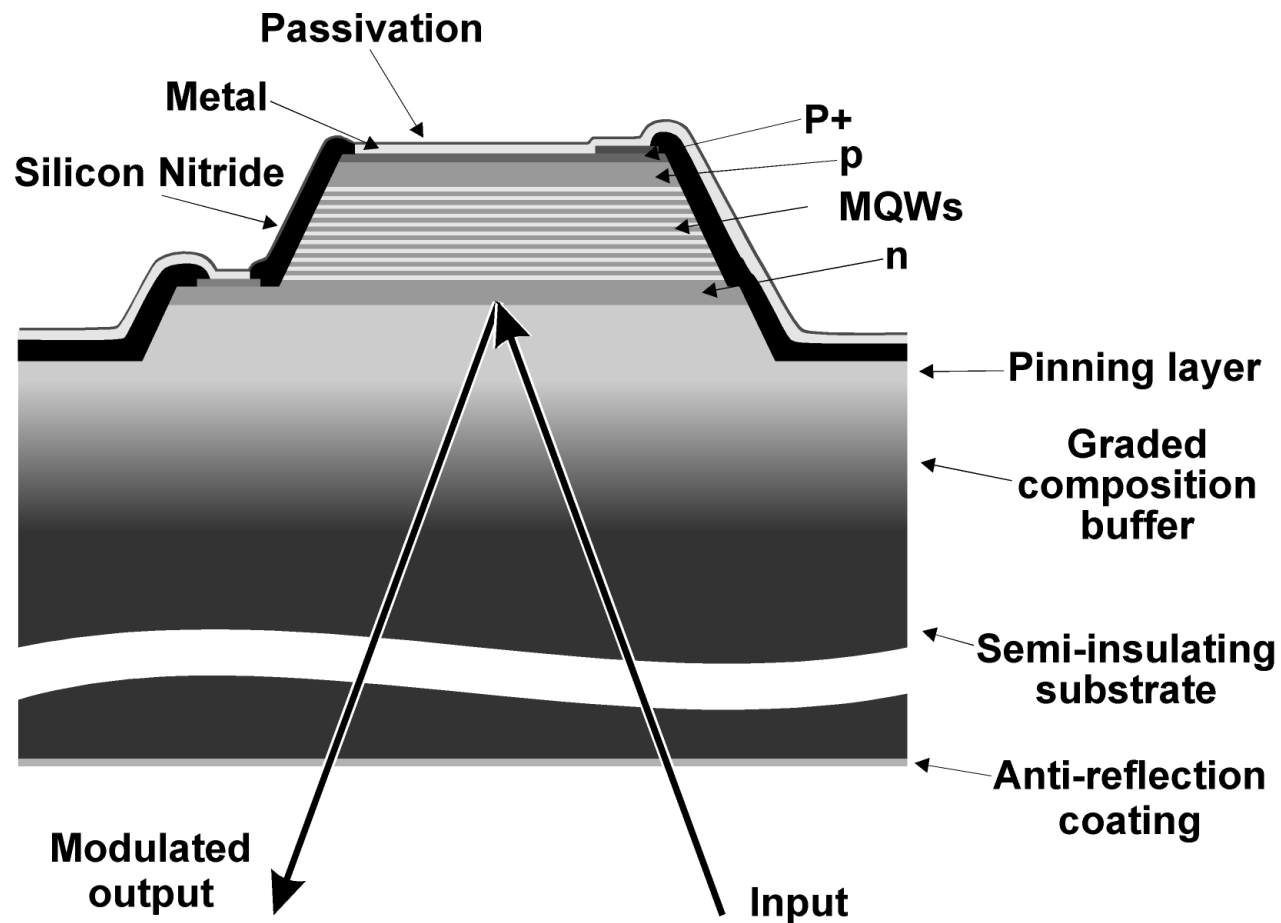
Typical speeds are $>1\text{GHz}$.

VCSEL array photograph
2.8mm

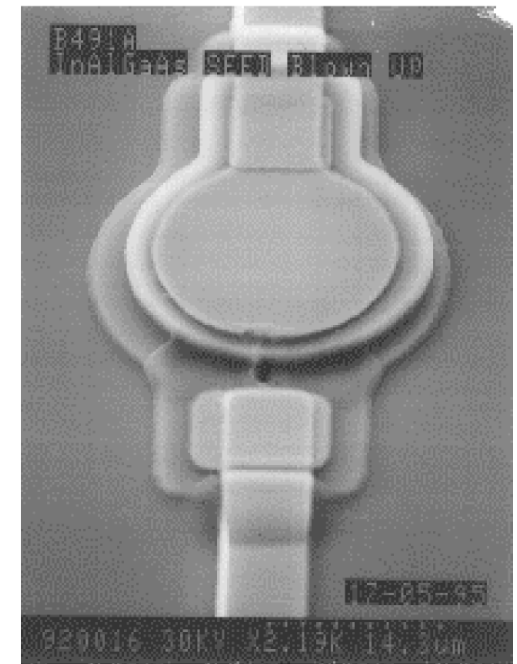


MQW Modulators

The MQW array does not produce its own output but modulates an input beam.



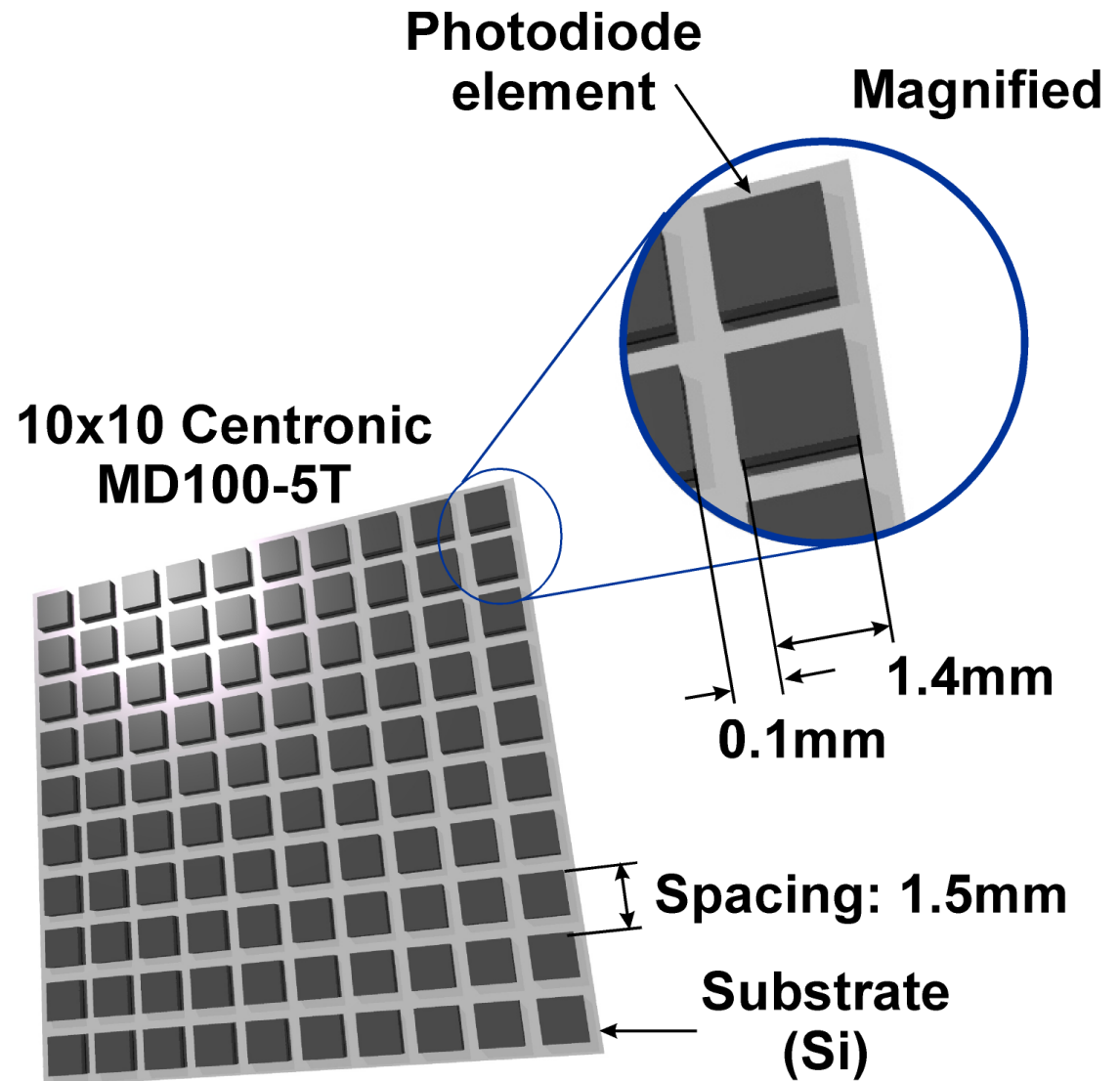
MQW Photograph



Detector Arrays

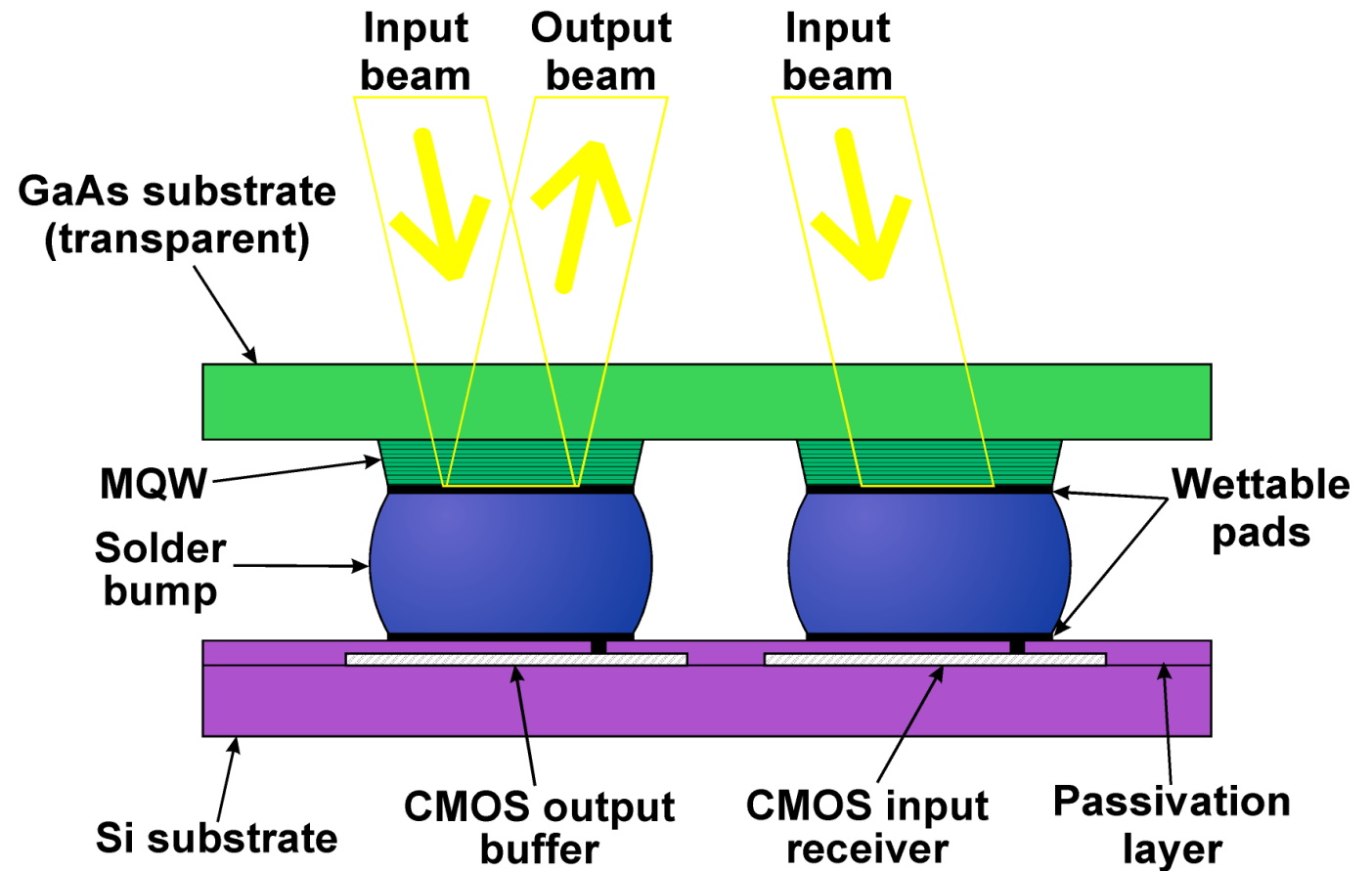
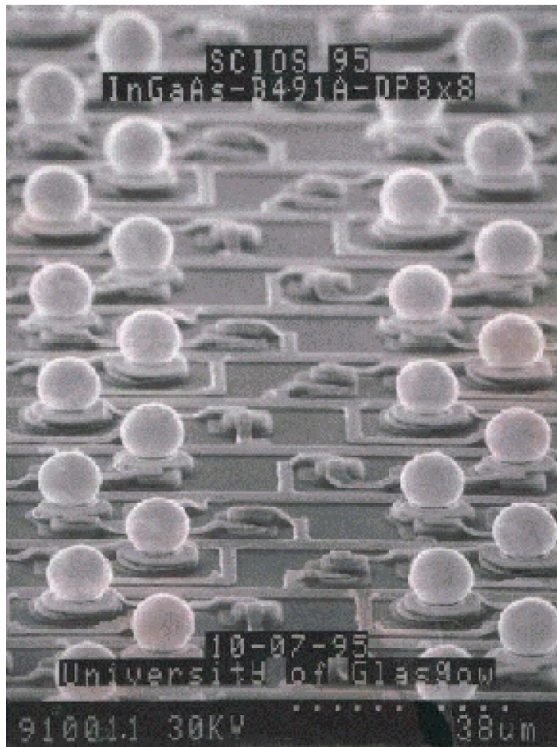
Photodetectors act as input devices and are currently available in a wide range off-the-shelf.

They are already responsive enough to handle input from any emitter (speed $>1\text{GHz}$): however the faster they are driven the more power they require.



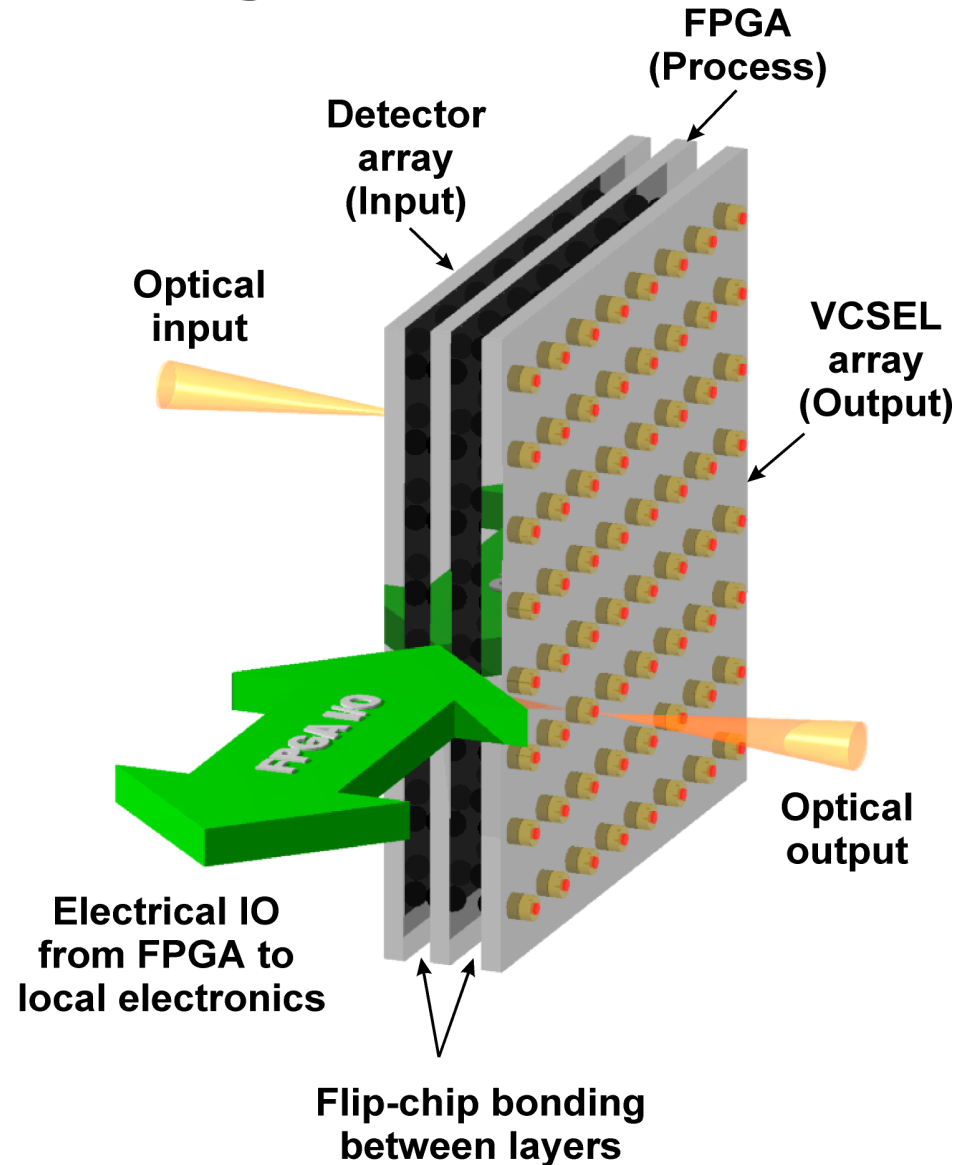
Flip-Chip Bonding

Solder bumps ready for flip-chip bonding process.



The “Inline” System

If the FPGA is dynamically reconfigurable then the inline system could be used for applications such as a telecommunications router or as an inline DSP-like system which could reconfigure its hardware to perform signal processing on an incoming data stream from a fibre bundle or free space.

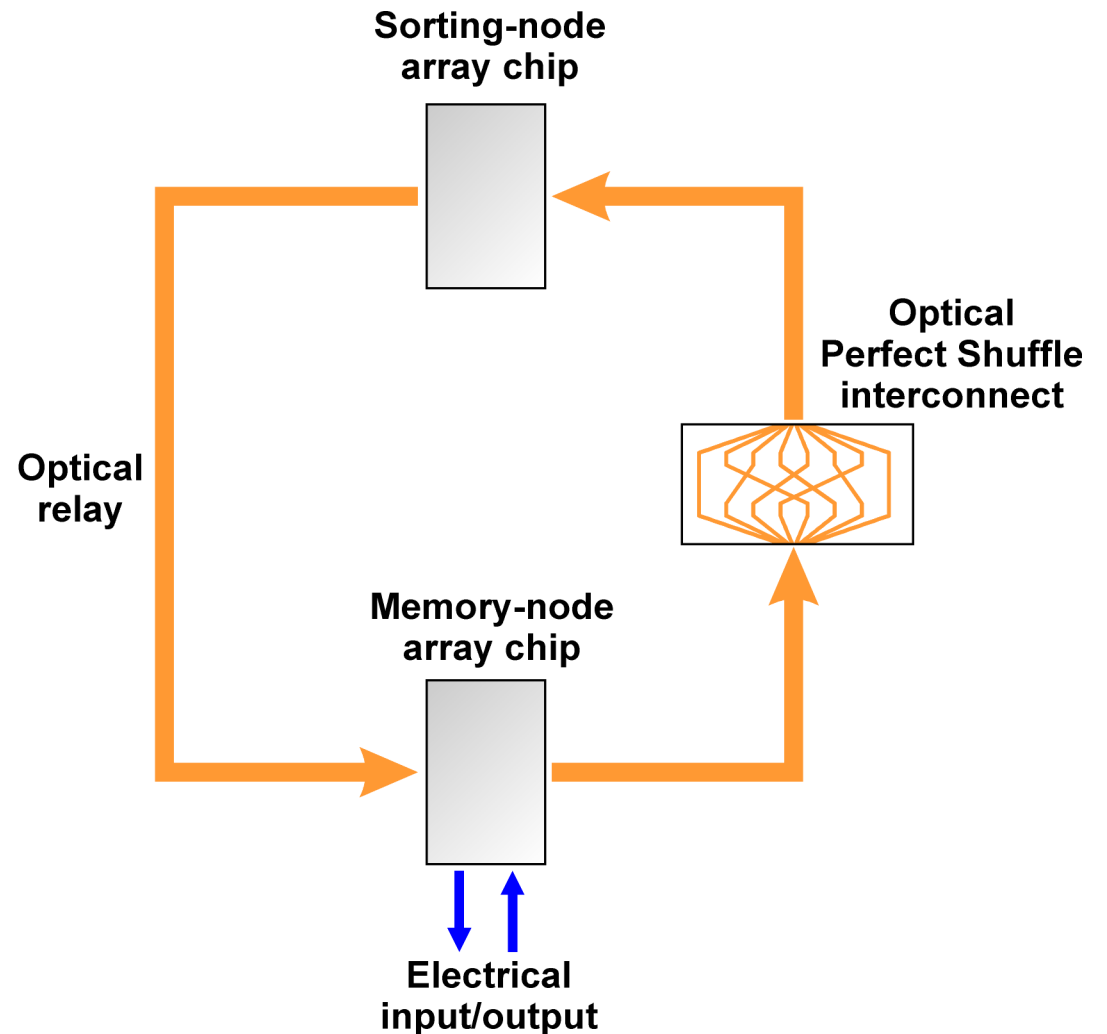


SCIOS Sorting Demonstrator

The architecture of the demonstrator utilises optoelectronics exploiting non-local interconnection: in this case the perfect shuffle.

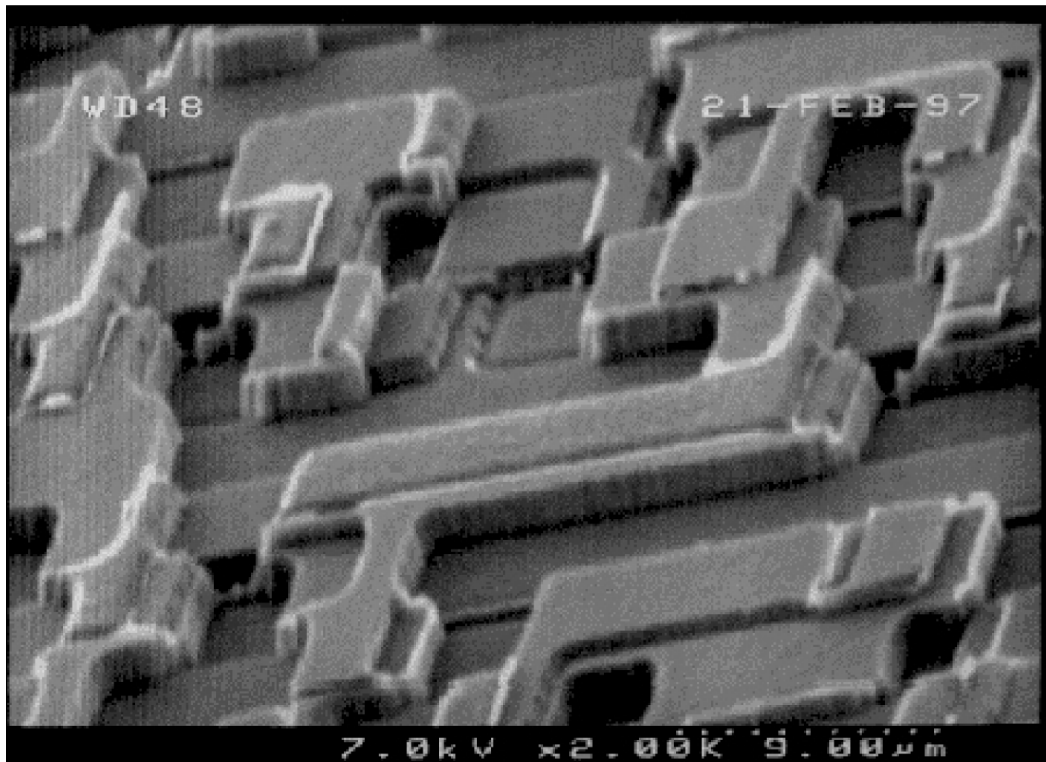
Right is a schematic of the sorting demonstrator.

The data to be sorted are entered sequentially into the processing loop through electrical I/O.

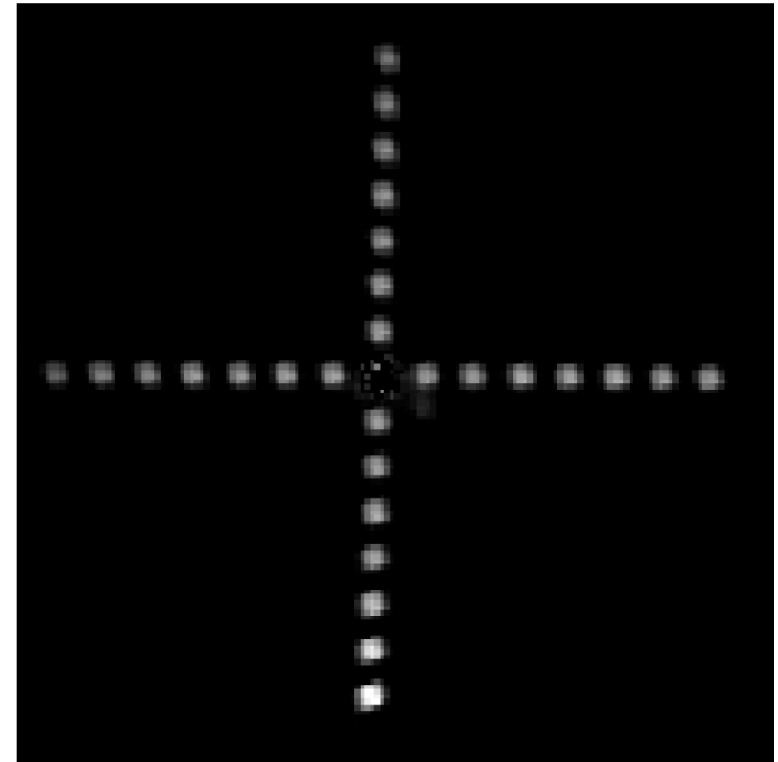


Diffractive Optic Elements (DOEs)

Sample DOE



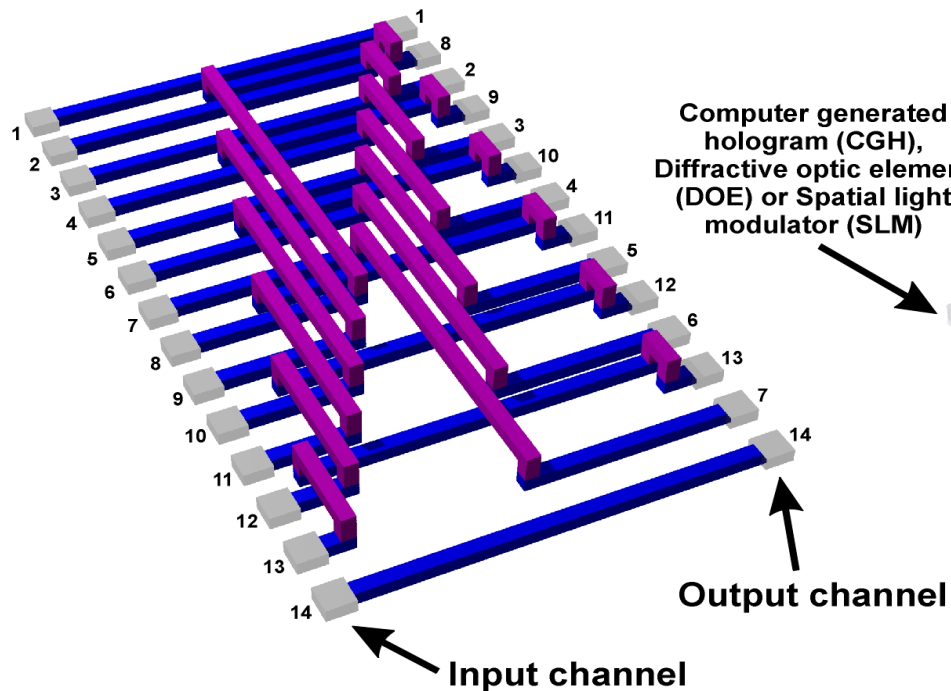
DOE Output
(Single beam input)



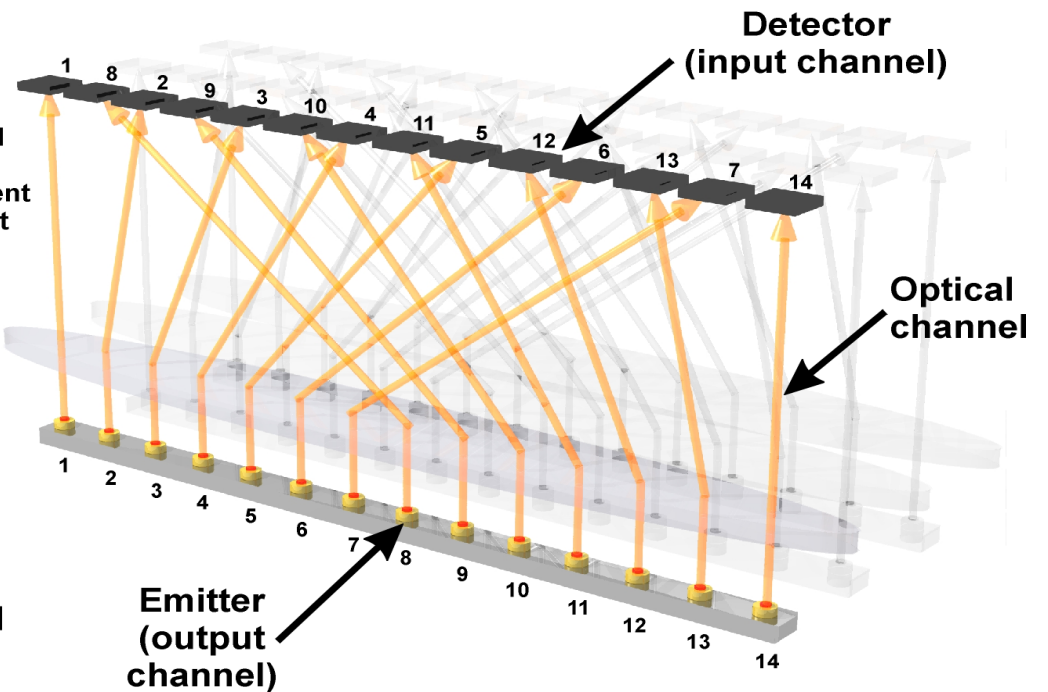
These elements are used as array generators and interconnection elements

Non-Local Interconnection

Two layer metallisation

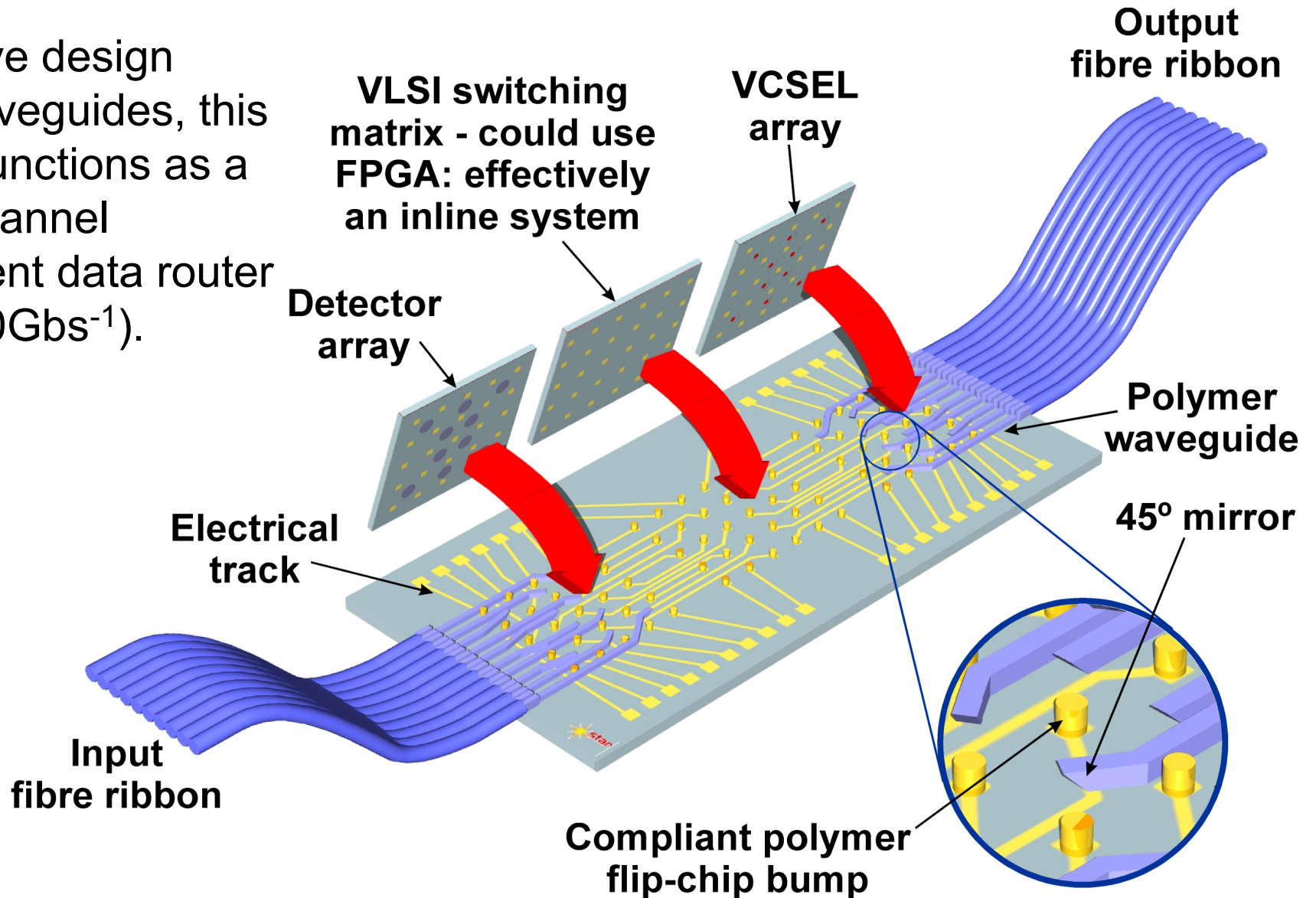


Optical implementation

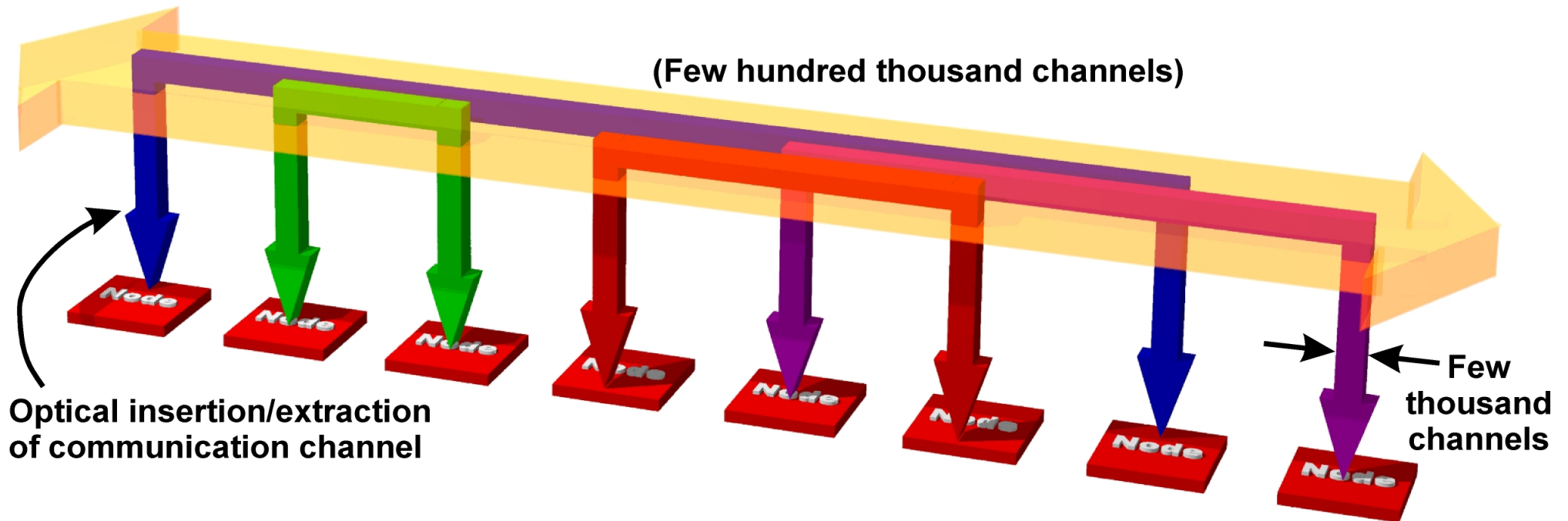


STAR Project

Alternative design using waveguides, this system functions as a 32x32 channel transparent data router (2.5 to 10Gbs⁻¹).



Optical Highways



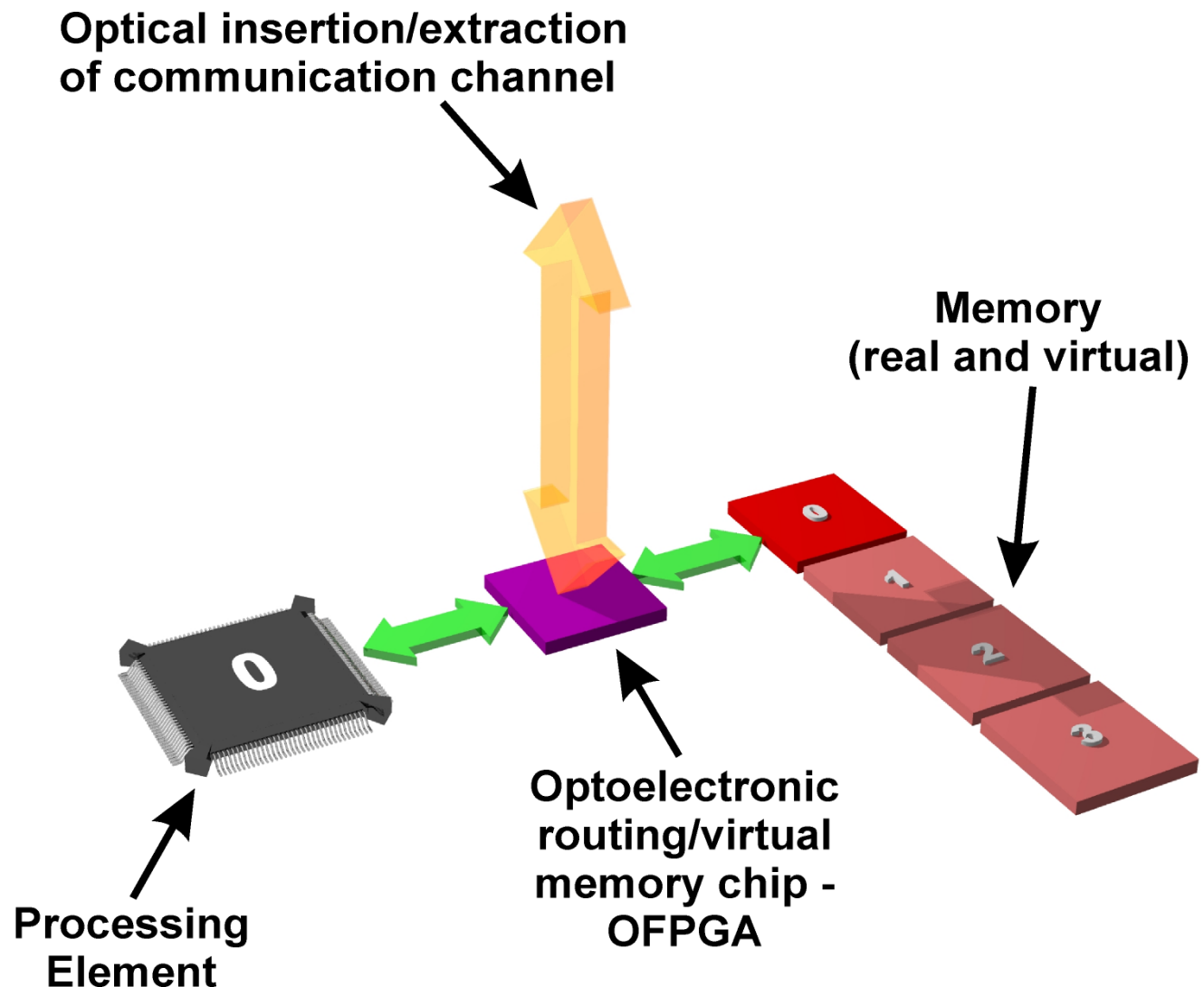
The concept of optical highways is to provide a general purpose multiprocessor harness with several thousands of channels passed node to node via an OFPGA interface.



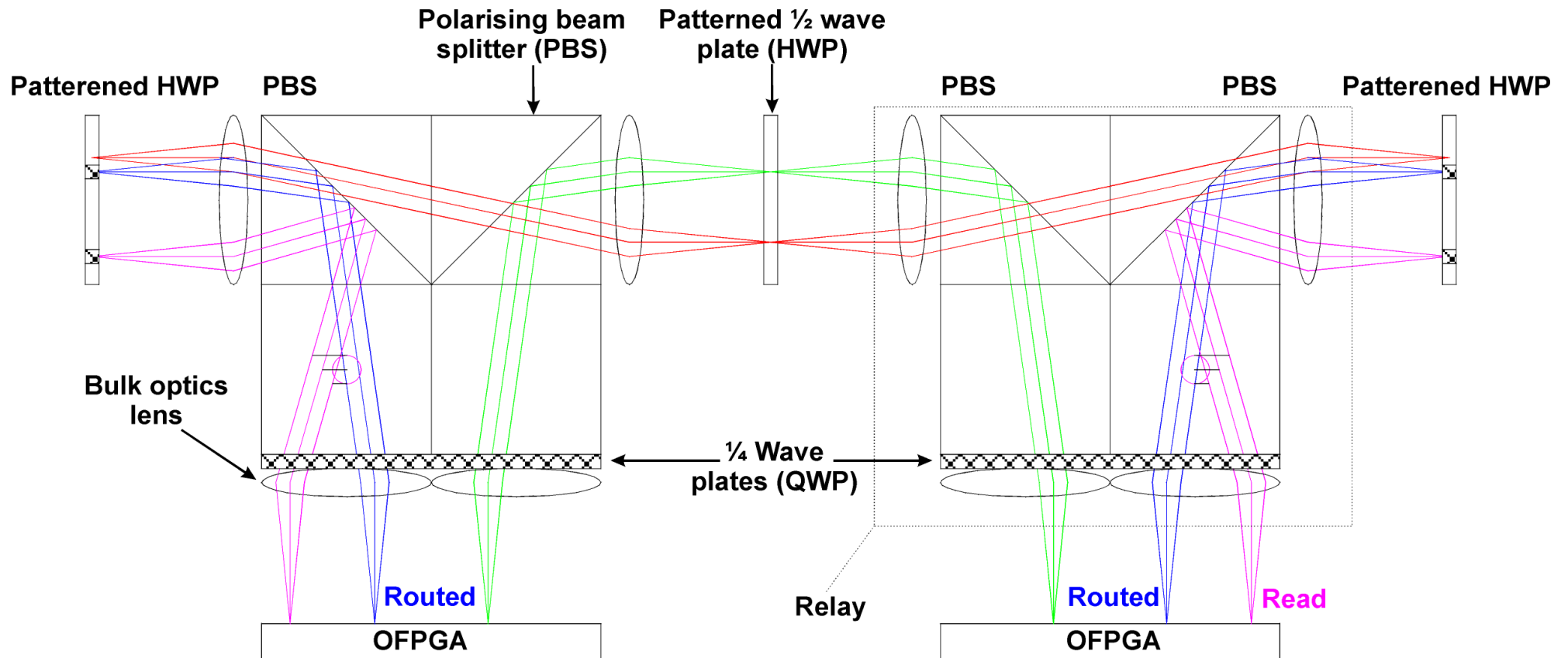
Optical Highway Node

Each node consists of a microprocessor, memory and cache and one or more OFPGAs to handle communications.

The role of OFPGAs in this architecture is to optimise the communications and processing in real time during execution of a range of algorithms.



Highway Implementation



The optical interconnect is 'hard-wired' using polarising optics to define computational topology.

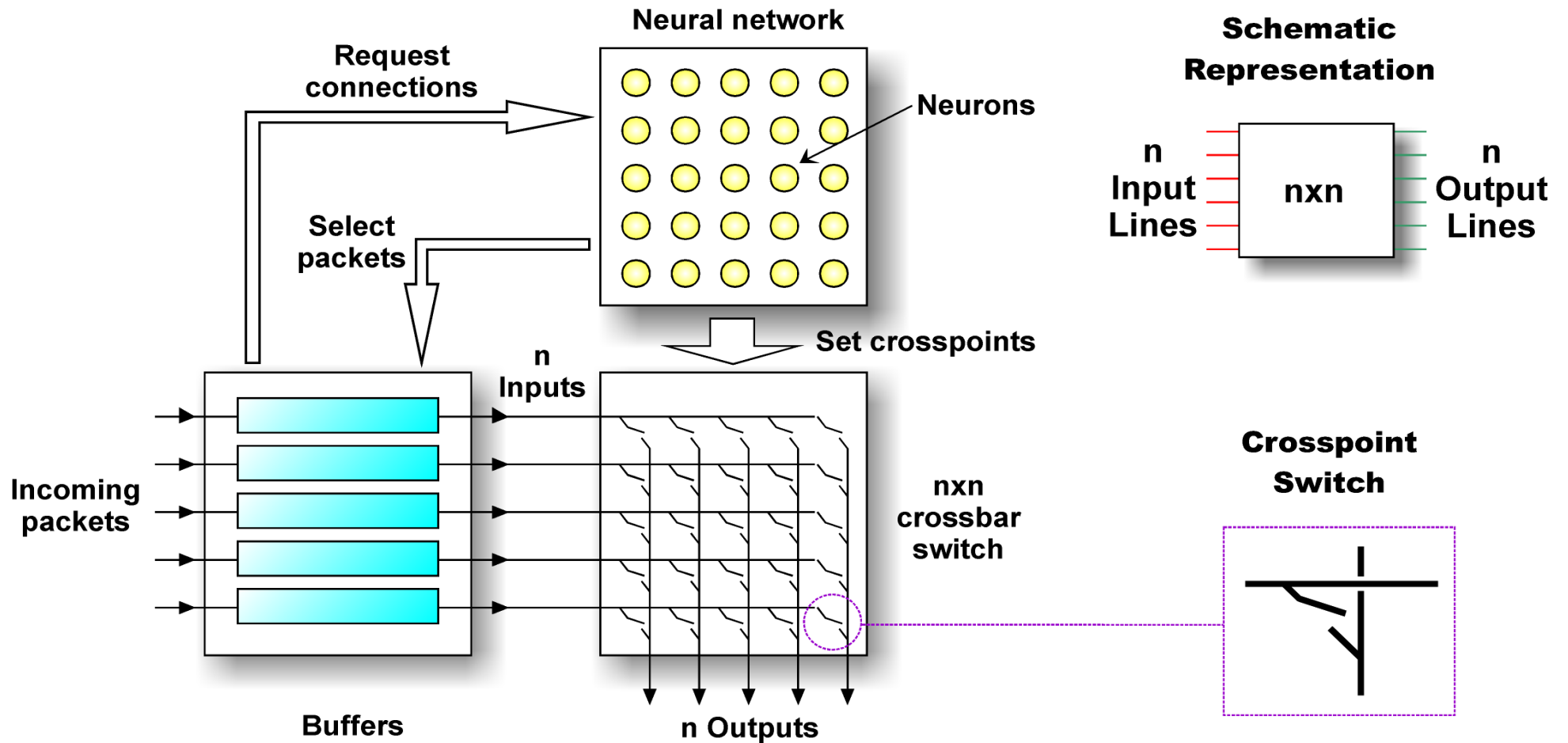


Optoelectronic Packet Switch Controller

- The next few slides examine a specific application which has led to the construction of a general purpose optoelectronic neural network.
- The design and motivation for the system will be discussed.
- Results will be presented from the first generation system.

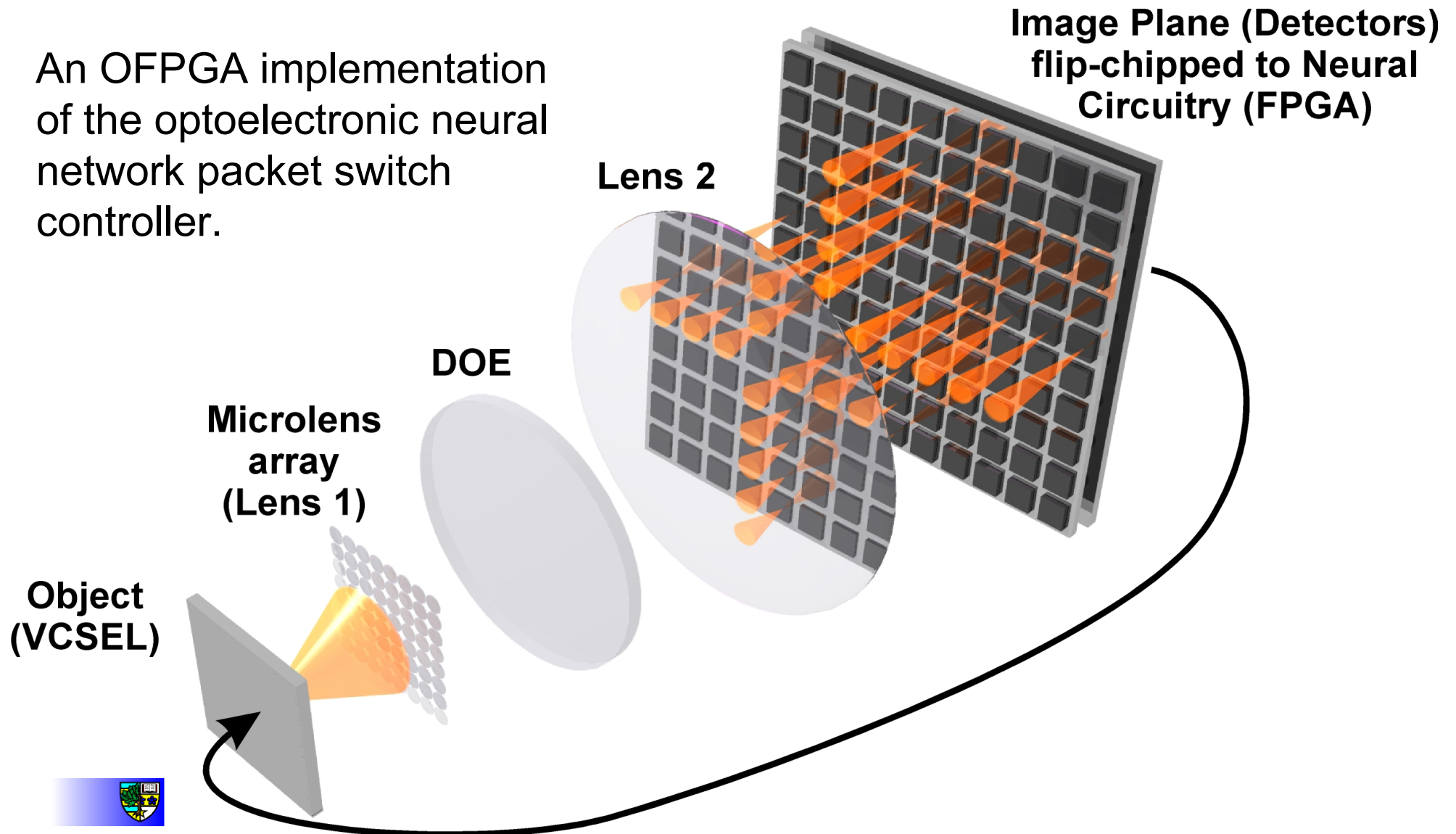


Crossbar Switching



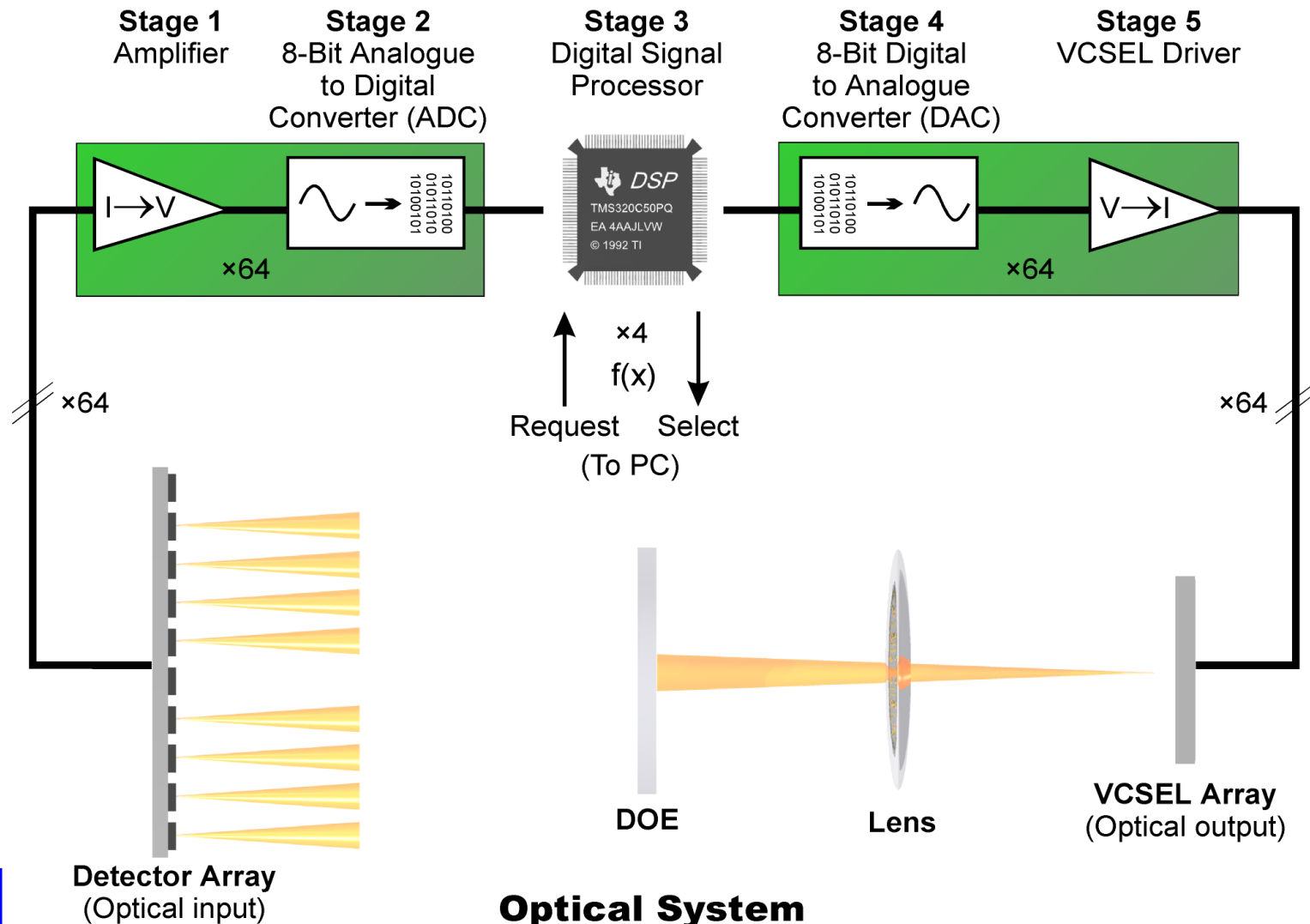
OFPGA Implementation

An OFPGA implementation of the optoelectronic neural network packet switch controller.



Current System

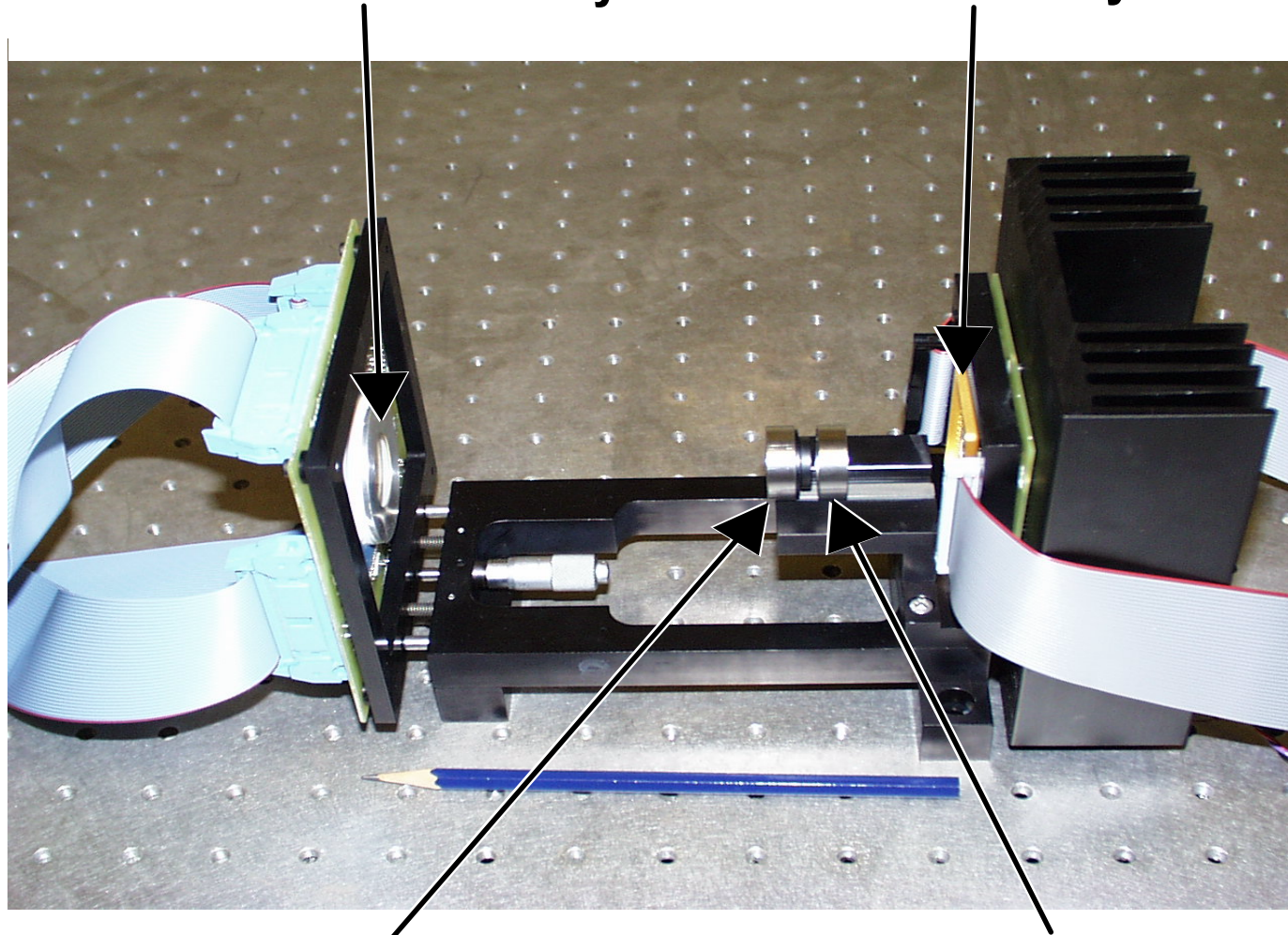
Electronic System



Optical System

Photodetector Array

VCSEL Array

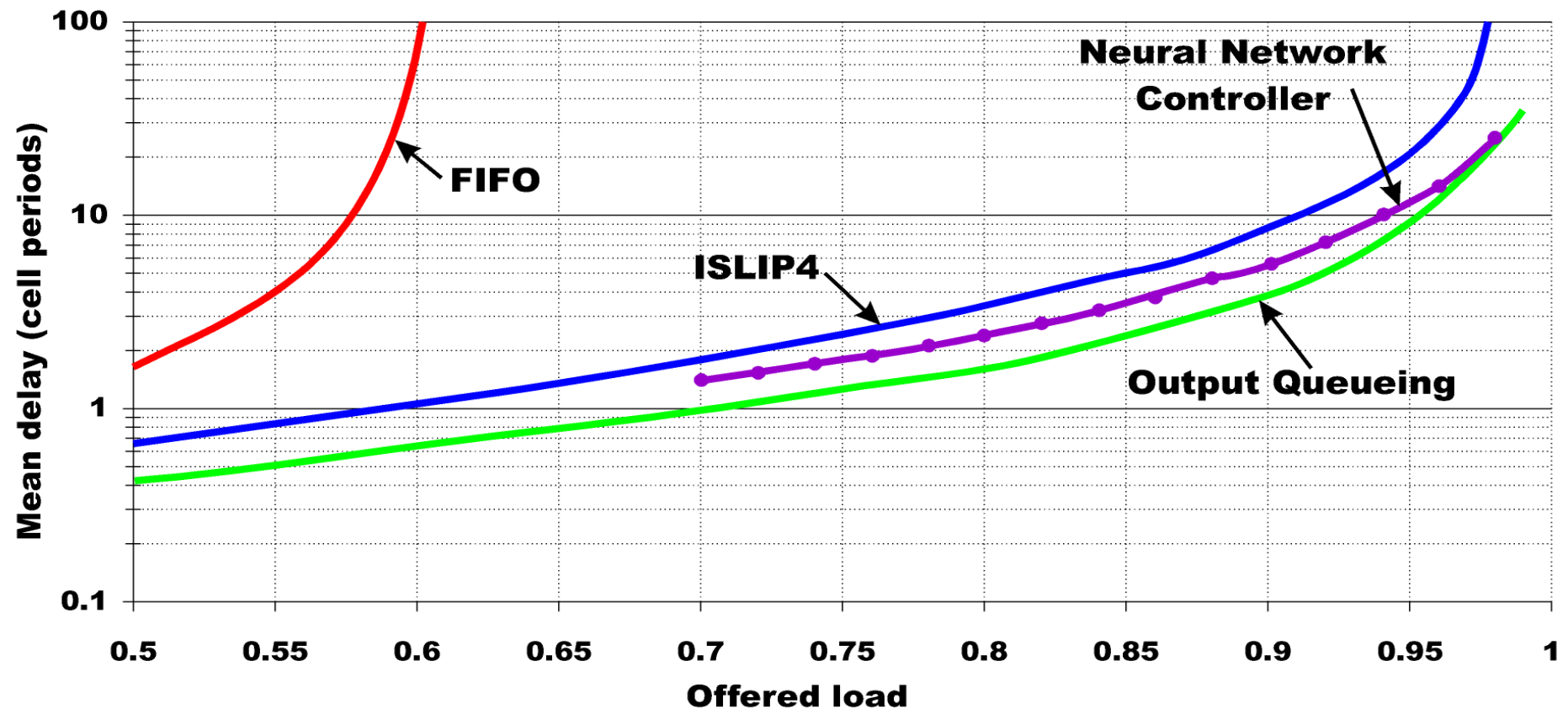


DOE

Lens



Performance



Engineering Issues

When using optics in any practical system, various factors must be considered.

- **Active effects:** $<1\text{Hz}$ thermal changes and component creep.
- **Static effects:** Tolerances in fabricated components could lead to misalignment in final system.
- **Adaptive effects:** Vibrational effects $>1\text{Hz}$ - e.g. 10kHz .

One way around these problems is to use active optic alignment or adaptive optics (AO) which perform measurement and correction of focusing and positional error in real time.

The commercial viability of such techniques is easily seen by looking at a CD player, now generally regarded as a disposable piece of machinery, which maintains focus and position of a light spot in real time on a rapidly rotating optical disk.

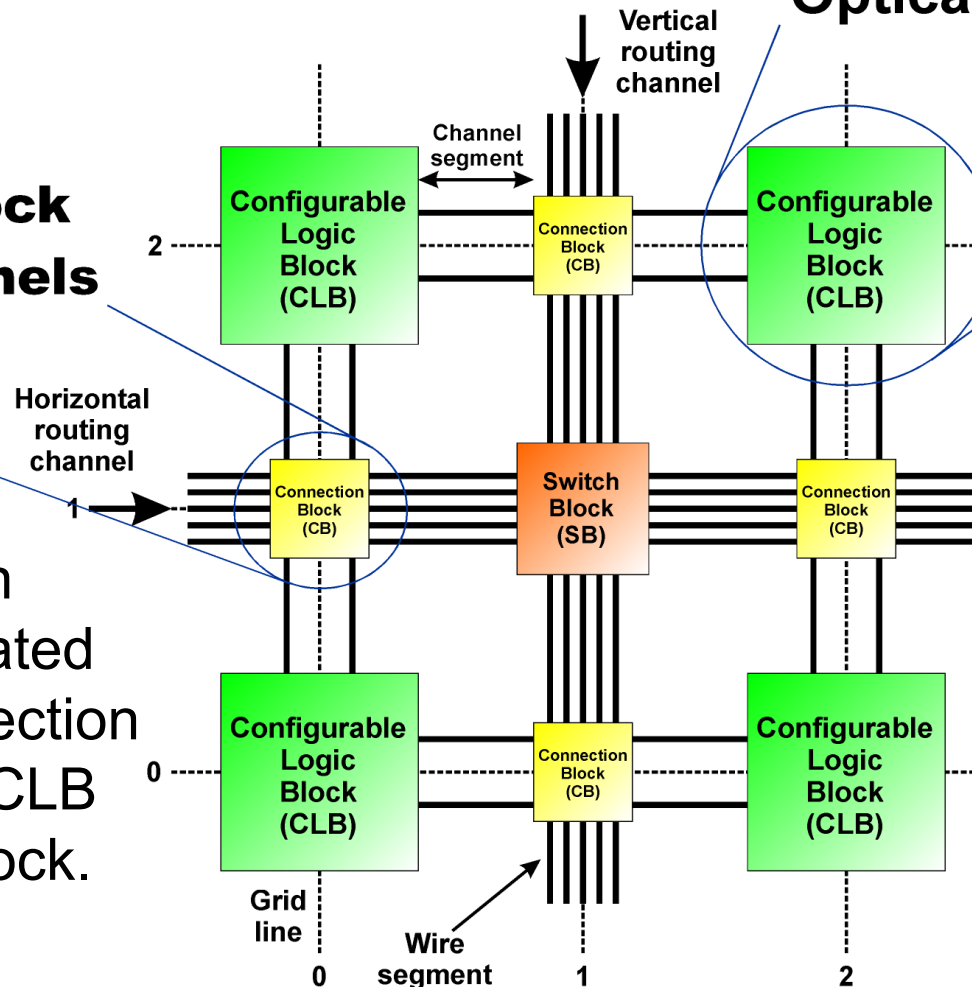


Sample Optical Interconnect Mapping

Connection Block to Optical Channels

Sample CLB with Optical Input Channel

A flip-chip connection point could be fabricated to allow optical connection either directly at the CLB or at a connection block.



Conclusions

There are essentially two reasons why optical interconnects are specifically of interest to dynamically reconfigurable FPGAs:

- **Bandwidth:** FPGAs are routed dynamically and any signal must therefore traverse both switching and routing blocks, each with an associated RC delay, to reach an I/O block. Optical I/O can relieve such bottlenecks.
- **Reconfiguration:** To make dynamically reconfigurable computing viable, new FPGA configurations must be downloaded at a rate which puts the component out of action for the shortest possible time period.

Optical Interconnects are not meant as a replacement but as an enhancement.

Without optical interconnection, be it through free-space or waveguide, dynamically reconfigurable computing will hit a premature performance ceiling due to bandwidth limitations.

