Using Optoelectronic Interconnects for Run Time Reconfigurable Arrays

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Outline

- Motivation: Optical interconnects for VLSI and reconfigurable architectures
- State-of-the-art
- Examples for reconfigurable optoelectronic architectures
- Summary

Motivation

- high integration circuit technology advances
- communication can not keep pace

  requirements: ~100 Gbit/s - 1 Tbit/s bandwidth in communication between memory-to-processor and processor-to-processor

- short distance optical interconnects offer solution
- chance: to integrate the performance of supercomputers in smallest space

Motivation

- Synergy Optics + Electronics
  - combine the strength of optics in data transport with the strength of electronics in data computation

  goal of interdisciplinary research topic

  Optics in Computing

- Role of computer science?
  - developing of architectures and algorithms well-suited to exploit efficiently optoelectronics
  - to verify the realisation of corresponding hardware

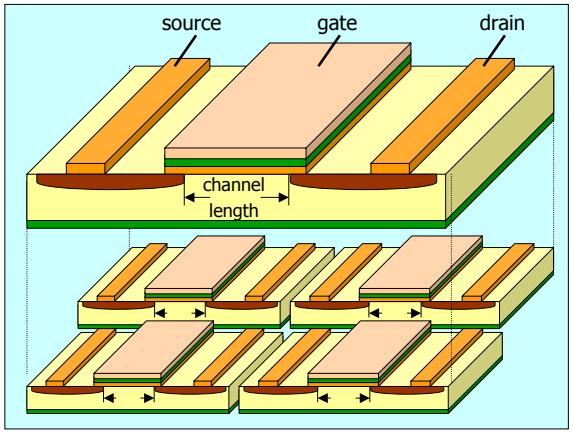
Motivation

- What are the benefits of optics?
  - high time bandwidth (per channel > 1 GHz)
  - high space bandwidth (> 1000 channels/cm²)
- Where can optics help?
  - clock distribution
  - broadcast and multi-point interconnections
  - dynamic reconfiguration
  - pin limitation

Motivation

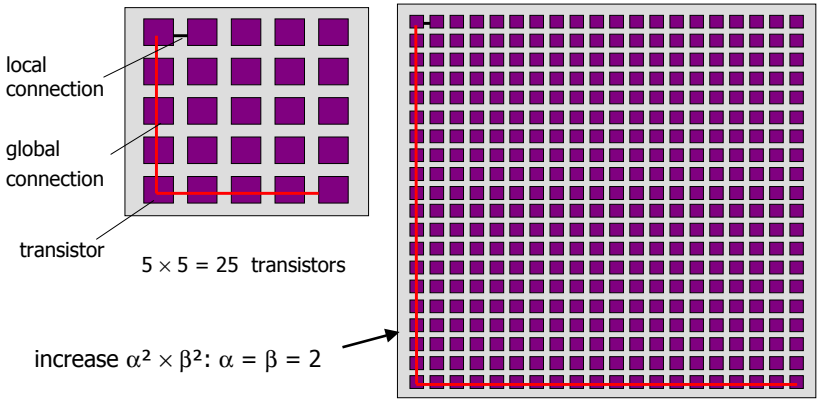
- square increase of number of devices due to scaling
  - example: scaling factor $\alpha = 2$

scaling about factor 2 ⇓ 4 times more transistors within the same area



Motivation

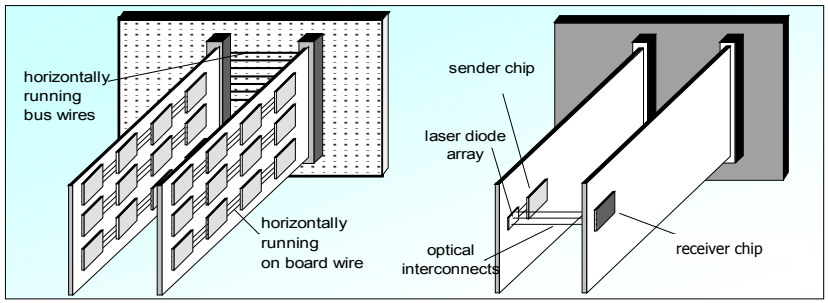
- increase in chip area
  - example: chip increasing factor $\beta = 2$



Motivation

- Benefit of optics: exploiting third dimension

wire based electronics 2-D | vertically running optical interconnects 3-D



- chip-to-chip area: 3-D optoelectronic VLSI
- architecture has to guarantee that advantage of third dimension still holds

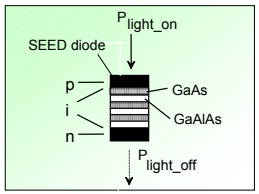
State-of-the-art

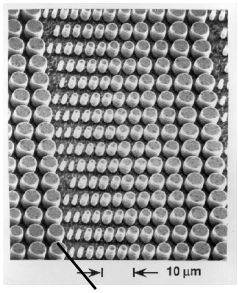
- Optical off-chip sending and receiving

Modulators (SEEDs)
- modulator and detector as well
- GaAs technology
- hybrid integration with CMOS

Arrays of micro lasers
- vertical surface emitting
- GaAs-Technologie
- hybrid integration with CMOS

Smart detectors
- photodiodes monolithically integrated with CMOS logic circuitry





VCSEL

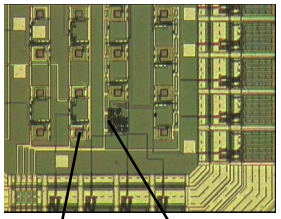
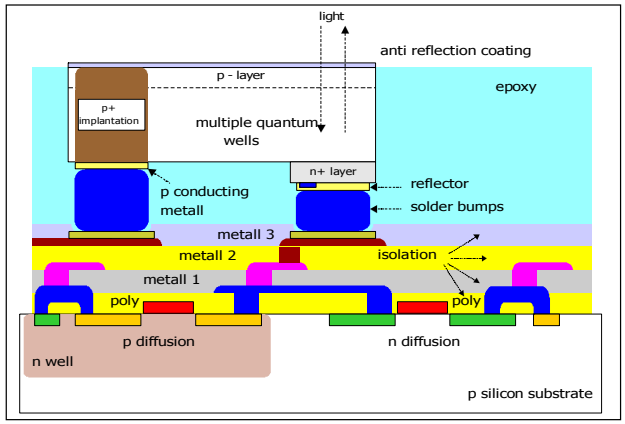


photo diodes

logic circuitry

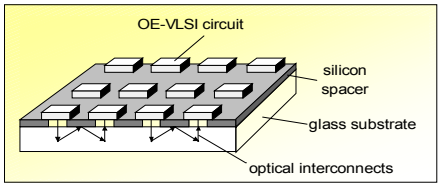
State-of-the-art

- hybrid integration of optoelectronic devices + CMOS
  - example for SEEDs: 2-D array of SEEDs is directly mounted on top of silicon circuit by flip-chip-bonding technique
  - controlled by output of CMOS circuit

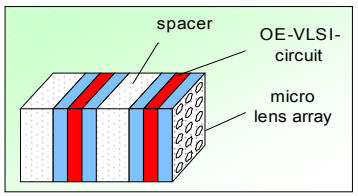


State-of-the-art

- integration optics and electronics
  - planar optics [FernUni Hagen; Jahns/Sinzinger/Gruber]



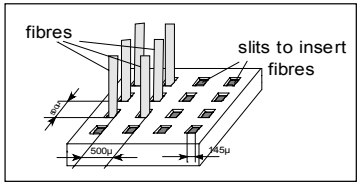
  - stacked optics [Uni Mannheim; Brenner/Krackhardt et. al.]

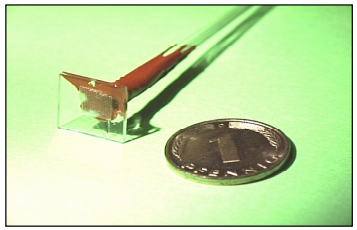


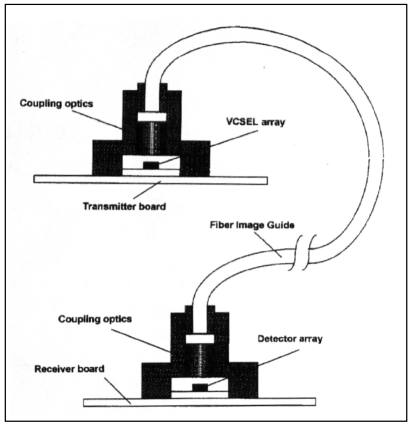
State-of-the-art

- fibre array
  [IPHT Jena; Bartelt/Hoppe]

[Maj/Kirk/Plant et. al.;
Applied Optics, 39, 5, Feb. 2000]

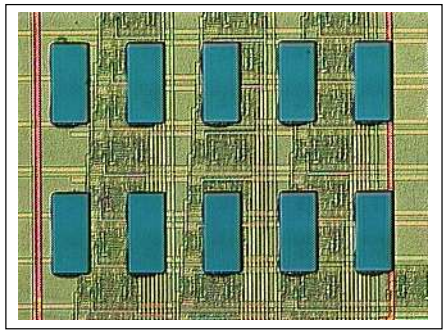






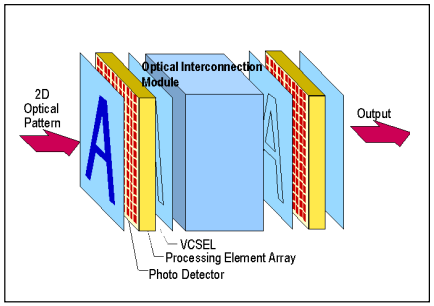
Examples for reconfigurable optoelectronic architectures

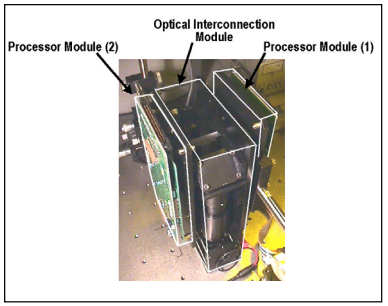
- Examples for reconfigurable optoelectronic architectures
  - optoelectronic reconfigurable PLD structures based on SEED-CMOS technique [Szymanski, McGill]



Examples for reconfigurable optoelectronic architectures

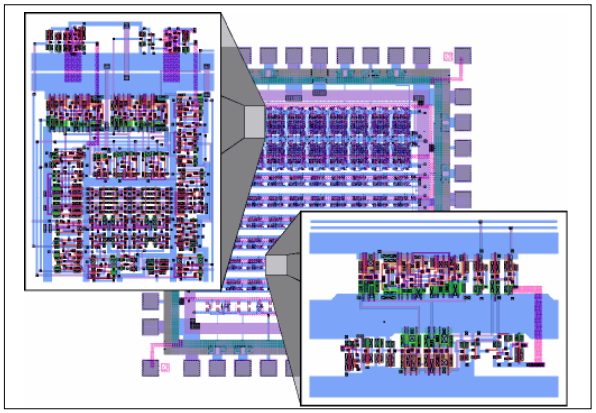
- OCULAR-II: dynamically reconfigurable optical interconnects [McArdle, Ishikawa; University Tokio]





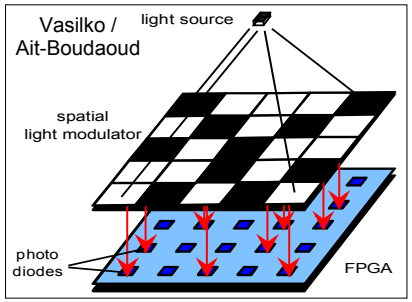
Examples for reconfigurable optoelectronic architectures

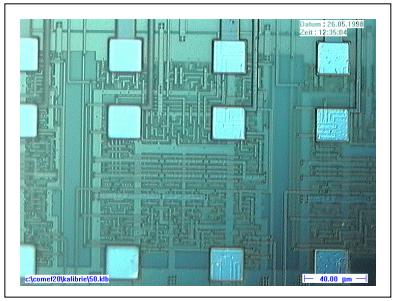
- Optically loadable look-up-tables
  - chip was realized in a foundry run organised by DARPA/Lucent
  - access time simulated in SPICE up to 250 MHz



Examples for reconfigurable optoelectronic architectures

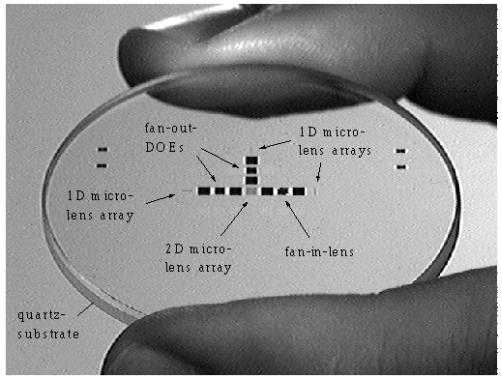
- parallel optical access allows fast, dynamic and partial reconfiguring
- reconfigurable look-up tables of size: 4×2 Bit
- 356 transistors on 24000µm² → ca. 4500 look-up tables / cm²
- parallel optical access allows reconfiguring of all look-up tables in ns





Examples for reconfigurable optoelectronic architectures

- Compact set-up as optical multi-chip module in planar optics [Gruber/Sinzinger/Jahns; University Hagen]



Examples for reconfigurable optoelectronic architectures

- Parallel optoelectronic processor for signal processing operations
  - calculation of standard functions is based on convergence algorithms
  - simple basic operations are sufficient
    - addition
    - bit shifting
    - bit check
    - table access
  - avoids area-consuming multiplication units
  - supports implementation of massively-parallel architectures
  - important for efficient implementation is table access

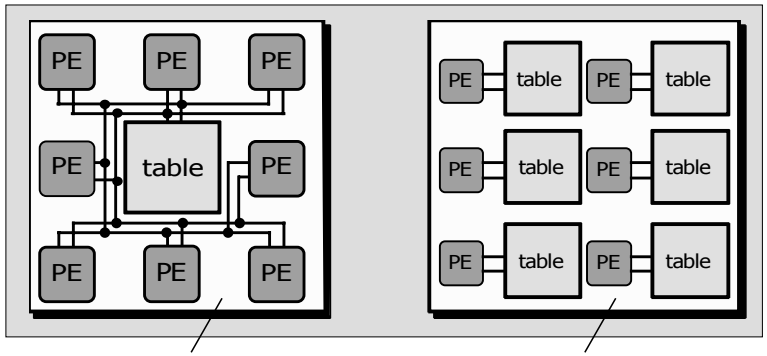
Examples for reconfigurable optoelectronic architectures

- developed convergence algorithms

function	iterative formulas	initial assignment	condition
$\cos\alpha$	$x_{i+1} = x_i \mp 2^{-i} \cdot z_i$ $y_{i+1} = y_i \mp \arctan 2^{-i}$ $z_{i+1} = z_i \pm 2^{-i} \cdot x_i$	$x_0 = \frac{1}{16467\ldots}$ $y_0 = \alpha$ $z_0 = 0$	$y_i \overset{?}{\geq} 0$
$\sin\alpha$	$x_{i+1} = x_i \pm 2^{-i} \cdot z_i$ $y_{i+1} = y_i \mp \arctan 2^{-i}$ $z_{i+1} = z_i \mp 2^{-i} \cdot x_i$	$x_0 = 0$ $y_0 = \alpha$ $z_0 = \frac{1}{16467\ldots}$	$y_i \overset{?}{\geq} 0$
$\arctan\alpha$	$x_{i+1} = x_i \pm \arctan 2^{-i}$ $y_{i+1} = y_i \mp 2^{-i} \cdot z_i$ $z_{i+1} = z_i \pm 2^{-i} \cdot y_i$	$x_0 = 0$ $y_0 = \alpha$ $z_0 = 1$	$y_i \overset{?}{\geq} 0$
$\frac{\alpha}{\beta}$	$x_{i+1} = x_i + 2^{-i} \cdot \alpha$ $y_{i+1} = y_i - 2^{-i} \cdot \beta$	$x_0 = 0$ $y_0 = 1$	$y_{i+1} \overset{?}{\geq} 0$
$\alpha \times \beta$	$x_{i+1} = x_i + 2^{-i} \cdot \alpha$ $y_{i+1} = y_i - 2^{-i}$	$x_0 = 0$ $y_0 = \beta$	$y_{i+1} \overset{?}{\geq} 0$
$\ln\alpha$	$x_{i+1} = x_i + \ln(1 + 2^{-i})$ $y_{i+1} = y_i - 2^{-i} \cdot y_i$	$x_0 = 0$ $y_0 = \alpha - 1$	$y_{i+1} \overset{?}{\geq} 0$
e^{α}	$x_{i+1} = x_i + 2^{-i} \cdot x_i$ $y_{i+1} = y_i - \ln(1 + 2^{-i})$	$x_0 = 1$ $y_0 = \alpha$	$y_{i+1} \overset{?}{\geq} 0$
$\sqrt{\alpha}$	$x_{i+1} = x_i + 2^{-(i+1)}$ $y_{i+1} = y_i - 2^{-i} \cdot x_i + 2^{-2(i+1)}$	$x_0 = 0$ $y_0 = \alpha$	$y_{i+1} \overset{?}{\geq} 0$

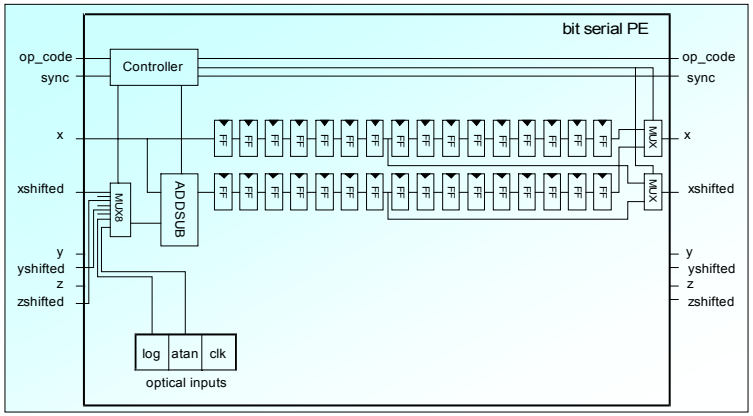
Examples for reconfigurable optoelectronic architectures

- parallel pure-electronic implementations failed due to effort for realizing the tables on chip



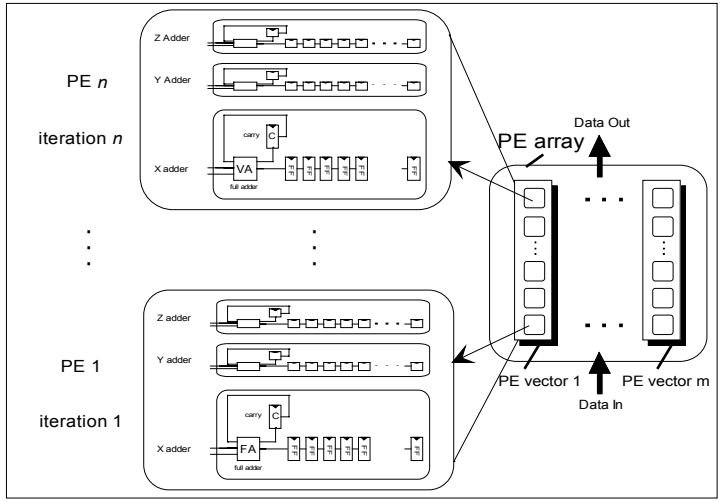
Examples for reconfigurable optoelectronic architectures

- Bit-serial architecture approach turned out as most efficient with regard to throughput performance
  - set-up of a single processing element:



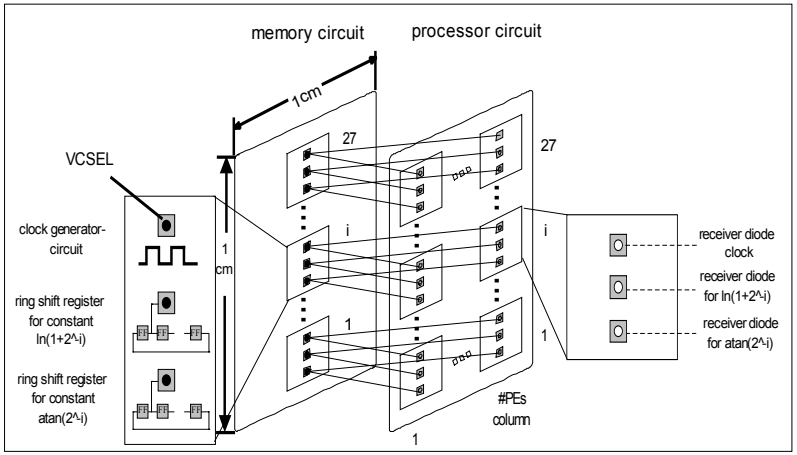
Examples for reconfigurable optoelectronic architectures

- Structure of the complete architecture



Examples for reconfigurable optoelectronic architectures

- Solution of efficient table access
  - parallel optical memory-processor interface

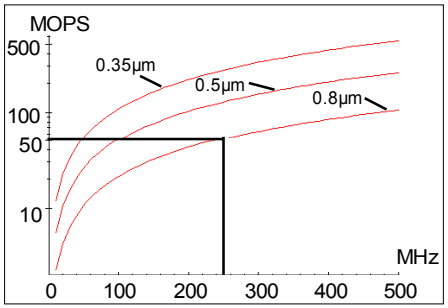


Examples for reconfigurable optoelectronic architectures

- Performance evaluation
  - CADENCE layout synthesis for 0.8µm CMOS process

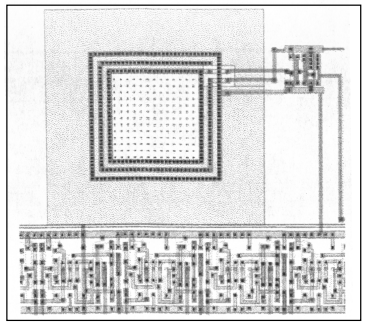
Parameter	bit serial 32 Bit
size PE	734×734 µm²
critical path length	3.66 ns

  - expected throughput performance



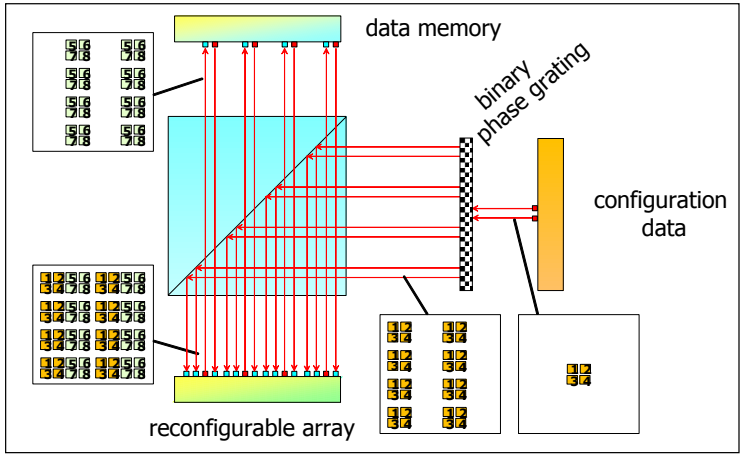
Examples for reconfigurable optoelectronic architectures

- test circuit designed as smart detector
  - diode geometry: 40 × 40 µm²
  - diodes (“optical input pins”) are arranged in 500 µm raster
  - designed for 0.8 µm BiCMOS process
  - speed: 166 Mbit/s for detecting and digitizing optical input
  - ideal case: 285 Mbit/s



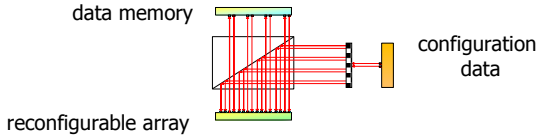
Approaches for run time reconfiguration with optical interconnects

- Scheme for optical run time reconfiguration on chip-to-chip area



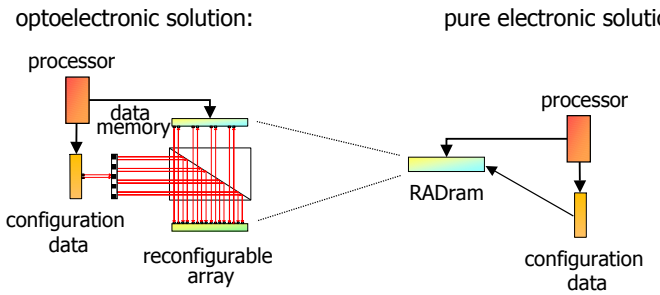
Approaches for run time reconfiguration with optical interconnects

- advantageous for smart memory approach
  - ”Active page model” [Oskin et. al.]
  - consists of processor and memory with reconfigurable logic (RADram)
    - data-intensive operations are shifted to the memory
    - computation is partitioned between processor and memory
  - active page : data page inclusive associative operation
  - Example:
    - gathering operands for a sparse-matrix operation
    - afterwards passing operands to the processor for execution
  - to perform such a gather function
    - matrix data gathering function are loaded into the RADram



Approaches for run time reconfiguration with optical interconnects

- benefits of using optical interconnects
  - 3-D VLSI approach allows separation of reconfigurable logic and memory
  - fast reconfiguring ~ns
  - parallel access allows reconfiguring of many cells within a few steps

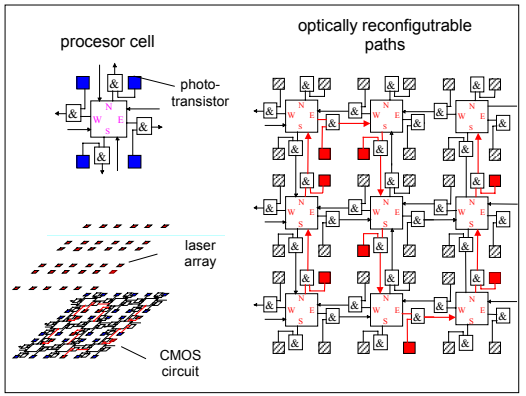


Approaches for run time reconfiguration with optical interconnects

- technology for memory circuitry and logic circuitry is different
  - technology is optimised for one application
  - this problem is not given in optoelectronics
    - both optimised technologies can be exploited
- optoelectronic approach has also benefits for other reconfigurable architectures (Silc/Robic/Ungerer: Processor Architectures)
  - MorphoSys (Univerity California at Irvine, Singh et. al., 1998)
  - RAW Machine (Waingold et. al., 1997)

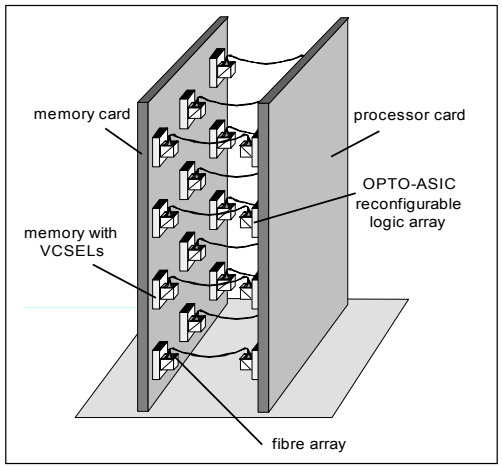
Approaches for run time reconfiguration with optical interconnects

- Chunky function unit architectures
  - coarse-grain reconfigurable computing
  - ALUs, registers, multipliers with programmable interconnects
  - optically reconfiguring of data paths in one cycle



Approaches for run time reconfiguration with optical interconnects

- Scheme for optical run time reconfiguration on board-to-board area



Summary

- benefits of optical interconnects in VLSI
  - solution for pin limitation
  - 3-D architectures
- state-of-the-art
  - devices for optical sending and receiving available
  - solutions for efficient integration techniques are on the way
- optoelectronic architectures with reconfigurable data paths
  - parallel optoelectronic digital signal processor presented
  - performance increase about factor 70 due to parallel optical memory-processor interface
- run time reconfiguration architectures
  - efficient solutions based on 3-D processor-memory coupling
  - dynamic reconfiguration of logic and interconnects